

Scalable Coil Sensors Readout for Eddy Current Testing Array Probes

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Abstract—This paper presents an advanced Eddy Current Probe (ECP) array tailored for layer-by-layer QC metal parts produced using PBF. The probe operates mounted on the PBF printer recoater, allowing layer-wise imaging to entirely reconstruct the metal part under production. The enhanced design for stimulation and acquisition allows a spatial resolution of 1 mm and a sampling frequency of 31.25 kHz. The layer wise scan approach eliminates the need for high penetration, leading to a stimulation frequency of 1 MHz. Moreover, the probe incorporates a sensor array featuring 240 coils for scanning wider metal areas aligning with the typical dimensions of the powder beds. The system successfully exhibits capabilities to scan PBF parts, achieving scan resolutions as low as 0.16 mm at 250 mm/s speeds.

Keywords—Eddy Current Testing, Powder Bed Fusion, Electromagnetic Geometry, Embedded Systems

I. INTRODUCTION

Additive Manufacturing (AM) of metallic objects is a technology that has earned tremendous popularity across several manufacturing sectors. Among others, medical, aerospace, automobile, and military are some predominant fields adopting the process [1]. The concept relies on “joining materials to make objects from a 3D model data, usually layer upon layer” [2]. It enables the production of complex geometries and shapes, providing unprecedented design flexibility [3].

The PBF is the industry’s most used form of metal AM due to its superior capability of making geometrically complex parts [1]. Aerospace frequently uses it to reduce component weight, lead times, and costs, such as in NASA, to produce rocket injectors [4]. The process relies on the layer-wise melting of a powder bed using a laser. It is a conceptually simple process, but the high heating and cooling rates it often results in objects with a rough surface and significant porosity [1].

The absence of a robust PBF process is one of the main barriers to the broader adoption of AM [3]. The recent interest in using PBF is increasing the need for QC [5] to overcome the process's inherent variability. There is a constant demand to maximize the part quality and consistency to obtain ready-for-use parts within the industry requirements [3], [4]. For this reason, in-situ monitoring is vital for the technology to mature by identifying and understanding defective conditions. It allows real-time control of the process parameters while manufacturing, enhancing the final piece's reliability.

Eddy Current Testing (ECT) is a well-established Non-Destructive Testing (NDT) technique used frequently for QC inspection in post-production scenarios. It is a contactless electromagnetic method inducing and sensing electrical current on conductive materials. The method allows for measuring material properties like conductivity and supports

detecting and characterizing surface and near-surface defects (e.g., porosity, cracks). The characteristics are suitable for integration into a layer-wise QC in-situ system able to provide the information of entire produced metal pieces with PBF. A few cases have emerged in recent years showing the ability to use it in such a context.

The ECT physical principle relies on the interaction between a magnetic field and the material under test. The procedure starts with a coil energized with an Alternating Current (AC) signal to create a primary magnetic field. Then, approaching the coil into the material causes its magnetic field to penetrate, inducing continuous and circular ECs in the material. These will generate a secondary magnetic field opposing the primary. The eddy currents will be affected in case of changes in conductivity, near-surface defects (cracks), or differences in thickness. The sensing coil impedance decreases according to the increased eddy current intensity [6]. So, measuring the coil impedance variation allows the sense of the EC and tracking the material modifications. The current or voltage signal is measured to monitor the impedance. This coil can be the same or a sense-dedicated one. Fig. 1 shows a representation of the physical principle.

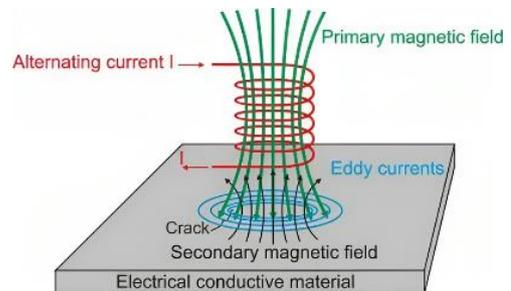


Fig. 1. Eddy current physical principle in [6].

This work resulted in a new one-dimensional ECP array specifically designed to mount directly on the recoater within the PBF 3D printer, as illustrated Fig. 2.

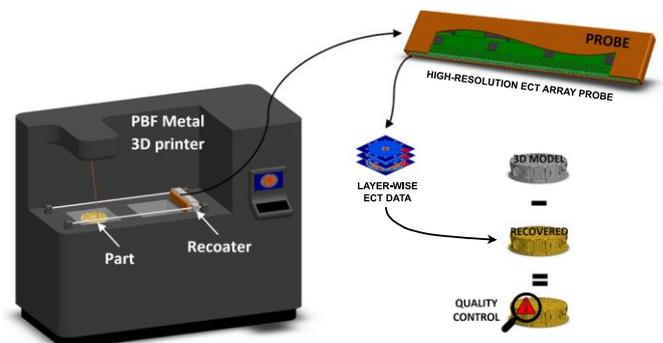


Fig. 2. ECT array setup goal for a PBF 3D printer, adapted from [7].

The presented setup allows performing layer-wise imaging. The probe scans the metal part each time the recoater moves to distribute the powder over the build platform. Meanwhile, as the recoater returns to its initial position and the laser melts the necessary regions, the probe transmits the material integrity data to the host computer to build and store the layer ECT scans. Upon completion of the metal part production, the host computer can reconstruct the entire specimen. This reconstruction will one day allow the printer technician to QC (inspect) the specimen compared with the 3D model.

This work presents the development of the system until the layer ECT scans storage, including essential studies regarding its geometry and operation. The probe takes advantage of the constant stimulation independent of the specimen properties and the sensing coils' position to enhance the sensitivity. The main improvements over the previously available probes include an enhanced spatial resolution allowing adequate characterization in a single recoater pass and high acquisition frequency, ensuring high scan resolution without constraining the recoater speed. Additionally, the probe incorporates a minimal signal demodulation circuitry, reducing temperature dependencies and channel mismatch. The encouraging results in a prototype version led to the design of a probe with an array length capable of scanning most of the powder bed sizes in the industry.

II. WIRELESS EDDY CURRENT ARRAY PROTOTYPE

Before the development of the ultimate probe, a demonstration kit was created to prove the concept of layer-wise imaging over PBF specimens. The Wireless Eddy Current Array Prototype (WECAP), depicted in Fig. 3, functioned as a development platform for studying, modeling, and validating the new concept.

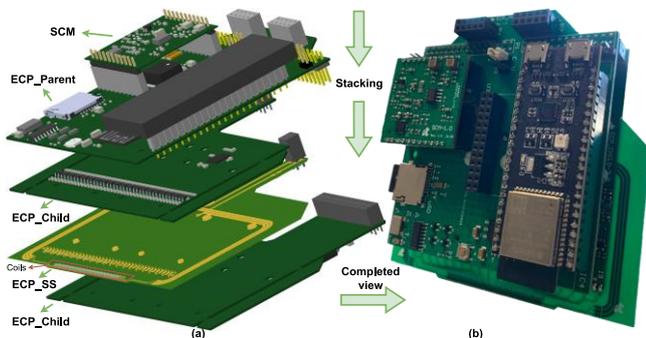


Fig. 3. WECAP PCB stackup (a) and real PCB view (b).

The WECAP development started by defining the stimulation and sensing topology. The prototype uses the reflection topology, where a single coil creates a uniform magnetic field, and sense coils to monitor the EC. The approach appears from the freedom to optimize the sensing and stimulation coils individually.

The innovative hardware concept utilizes a four-PCB stackup, ensuring a compact shape. ECP_Child integrates AFE and digital cores for signal acquisition, while SCM independently drives the 3-turn stimulation coil in ECP_SS, ensuring uniform and strong magnetic field. ECP_SS houses the sensing coil array, minimizing distances to stimulation and edges. ECP_Parent serves as the interface for all PCBs, facilitating communication and integration.

A. System Architecture

The proposed system considers the industry requirements and the existing standards to produce a powerful enough probe to scan PBF-produced parts. The overall architecture of the proposed system is presented in Fig. 4.

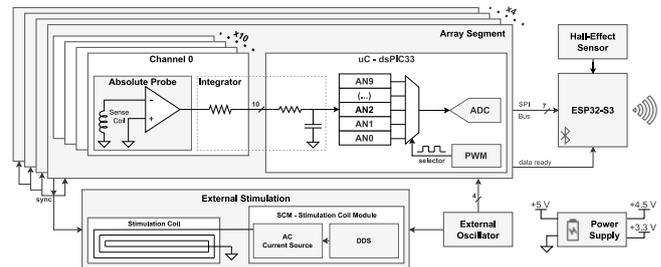


Fig. 4. WECAP block diagram.

The probe architecture stands out for its minimal AFE in each channel, reducing the overall footprint and minimizing the temperature dependency while achieving a spatial resolution of 1 mm. Simplification in the probe channels circuitry appears from the stimulation and sensing electromagnetic geometry design and the external stimulation using a powerful AC current source. The probe incorporates 40 sensing coils, allowing scanning PBF layers with a length of 40 mm.

The high-frequency readout is possible using four high-speed dsPIC33CK64MC10 microcontrollers. The WECAP is an wireless device, battery-powered with data acquisition through Bluetooth Low Energy (BLE) using an ESP32-S3. The digital domain elements all share an external oscillator for synchronization. The Hall-Effect sensor is an optional feature for scan position purposes. The overall specifications of the system are listed in Table I.

TABLE I. WECAP OVERALL SPECIFICATIONS

Dimensions	100x100 mm
Spatial Resolution (Coils pitch)	1 mm
Scan length	40 mm
Scan resolution (250 mm/s)	0.48 mm
Sampling rate	31.25 kHz
Readout Frequency	520.83 Hz
Stimulation frequency	1 MHz
Array Segment clock	180 MHz
Interface clock	240 MHz
Supply Voltage	5 V
Power Consumption	2.748 W

B. Stimulation

Traditionally, a constant voltage source drives the coil, but the current flowing might not be constant due to impedance variations. The impedance might change according to the material being tested. Considering the example in Fig. 5, when the WECAP starts passing over the ferromagnetic part, the electrical conductivity and magnetic permeability difference would change the stimulation coil impedance. The scan of the

non-ferromagnetic part would suffer variations due to the primary magnetic field variations.

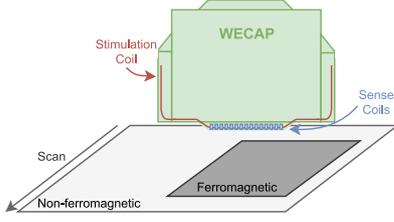


Fig. 5. Scan example for stimulation coil with impedance variations.

In order to provide a constant current flowing through the coil to ensure a stationary and material-independent magnetic field, a Stimulation Coil Module (SCM) was developed. It is a voltage-controlled current source with high output capability, providing higher detection sensitivity since only the secondary magnetic field is expected to change with the surface inspection. A Direct Digital Synthesis (DDS) chip generates the sinusoidal signal at a fixed frequency of 1 MHz. This frequency results in a standard depth of penetration around 400 μm for stainless steel 316, allowing for scanning the surface layer and the preceding layers, considering the 60 μm thickness of each LB-PBF layer [8]. Fig. 6 presents the stimulation schematic.

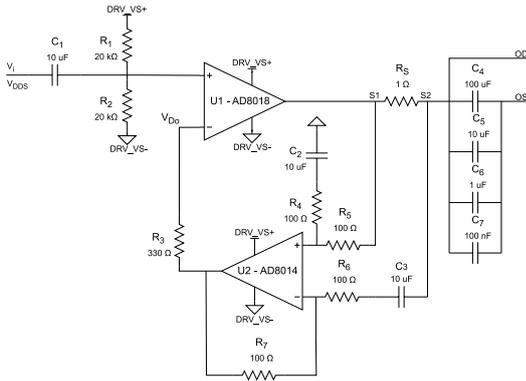


Fig. 6. Stimulation driver schematic.

A current source ideally provides an amplitude fixed current signal independently of the load characteristics. The design has a high-power Operational Amplifier (OPAMP) in the forward network and a subtractor topology in the feedback. A deeper analysis is beneficial to understand, starting with the subtractor equation

$$V_{D_0} = k_D(V_{S1} - V_{S2}), \quad (1)$$

with k_D being the subtractor gain equal to $\frac{R_7}{R_6} = \frac{R_4}{R_5}$. The equation can be simplified as

$$V_{D_0} = k_D R_S I_o, \quad (2)$$

regarding the output current and sense resistor.

Considering the virtual short and the feedback network sensing the voltage drop on R_S , the OPAMP output voltage will equal the input voltage, $V_{D_0} = V_{DDS}$. This results in the output load current being

$$I_o = \frac{V_{DDS}}{k_D R_S}, \quad (3)$$

controlled and proportional to the input voltage. If the load assumes a different value, the voltage sensed changes making the OPAMP adjust the output voltage, and the load's current is maintained within limits.

Since the current source is voltage-controlled, a resistor in DDS circuitry plays a significant role in defining the current in the stimulation coil by changing the DDS voltage. According to the values of the resistors in use, the relation is 1V/1A, meaning that 350 mV at the DDS output leads to a 350 mA of peak current flowing through the load coil.

The SCM performance was characterized according to the phase margin and bandwidth. Using a resistor as a load, the SCM has a very robust performance, but the scenario changes when using a coil. The phase margin for lower inductance values does not comply with the 45° rule of thumb. In contrast, it improves with high inductance coils, but the bandwidth is low, and the resistance value is too high, making these unsuitable for providing high currents.

The strategy to overcome the inductance problem is to place a resonant series output capacitor (C_S) to cancel out the reactive components seen by the current source at the stimulation frequency, as shown in Fig. 7.

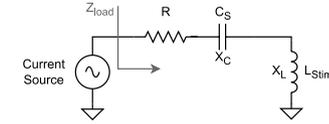


Fig. 7. Series resonance circuit for enhanced stimulation.

The following equation gives the load impedance:

$$Z_{load} = R + jX_C + jX_L, \quad (4)$$

At the resonant frequency ($f = 1/2\pi\sqrt{LC}$), the reactances $X_L = \omega L$ and $X_C = -1/\omega C$ are equal and opposite, canceling each other, and the load impedance becomes purely resistive (R). The new impedance at resonance is the lowest, and the current source can deliver higher currents since the voltage necessary to drive is lower.

C. Probe Readout

The probe readout refers to the AFE comprising the necessary hardware for adequately handling the sense coil signal. The AFE guarantees maximizing the signal according to the microcontroller characteristics. The hardware is equal for each coil (channel) to minimize the dissimilarity.

The AFE initial stage is an inverter amplifier. This stage biases the coil signal to mid-supply. The amplification enhances the signal's dynamic range to use the Full-Scale Range (FSR) of the next stage, ADC. Fig. 8 presents the first stage amplifier schematic.

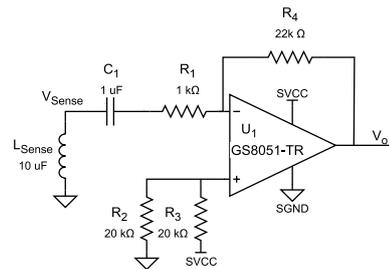


Fig. 8. Sense coil inverter amplifier schematic.

The most crucial component in the stage is the sensing element. The coil is a standalone sensor used only for sensing. The primary goal is to ensure the lowest pitch possible, leading to the coil package 0402 establishing a spatial resolution of 1 mm.

The amplifier topology is AC coupled, meaning only the time variant signal undergoes amplification. The C_1 guarantees only to pass the AC signal, and the voltage divider with R_2 and R_3 forces the OPAMP to replicate the mid-supply at its output. The output voltage follows the Equation below

$$V_o = \frac{R_4}{R_1} V_{Sense} + \frac{SVCC}{2}. \quad (5)$$

According to the resistors' values, the gain is 22. However, individually adjusting the gain for all 40 channels would be time-consuming. As a more efficient alternative, the approach involved precisely adjusting the stimulation current using a single resistor.

The AFE final stage is the Synchronous Demodulation & Sampling (SDS) and defines the interface of the previous amplified sensing signal with the microcontroller ADC. In this phase, the signal demodulation occurs through synchronous sampling. Fig. 9 represents the interface design.

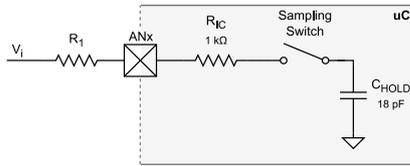


Fig. 9. Stimulation signal microcontroller interface schematic.

The approach developed involves modifying the internal microcontroller ADC Sample & Hold (S&H) circuit operation concept. Using R_1 with a tuned value allows for modifying the time constant (τ) made with the capacitor C_{HOLD} to perform an integration process, as the equation below describes

$$V_{Sample} = \frac{1}{\tau} \int_0^t V_i dt, \quad (6)$$

with $\tau = (R_1 + R_{IC})C_{HOLD}$, valid for $t \ll \tau$. To understand the method entirely, Fig. 10 illustrates a generic example. The V_{Sense} is the signal after amplification (input of the SDS), the S&H is the sampling switch activation signal, and V_{Sample} is the signal on the C_{HOLD} .

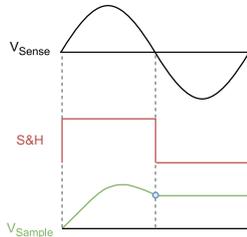


Fig. 10. SDS generic example.

The example only shows a single cycle of V_{Sense} , but the process keeps occurring as long as S&H asserts to acquire measures. Usually, every time the S&H goes high, the signal on the capacitor would be a replica slightly shifted from the original signal. Nevertheless, with the design above, the result is an integration of the positive half-cycle of V_{Sense} . The concept resides in establishing a fixed point (blue dot) for

sampling. E.g., When having the WECAP statically over a material, the acquired voltage is constant, but when scanning, it changes proportionally with the material conditions.

During several tests on exploring the possibilities of R_1 values and S&H activation, and the conclusion was different. The optimal performance was achieved with a low integration factor, using only R_{IC} and activating the S&H to acquire sample points of V_{Sense} with 69° or 249° of phase. Essentially, the sample point aligns with either the negative or positive peak.

D. Firmware - Probe readout

The readout concerns all the microcontroller operations required for acquiring the sensing coil signals. The architecture developed enhances the readout frequency by handling most of the operations through hardware peripherals. Fig. 11 illustrates the readout stages.

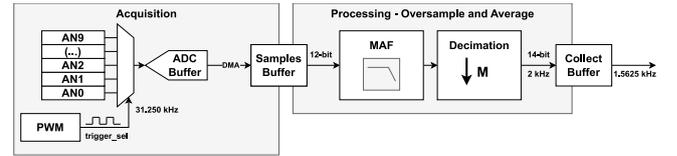


Fig. 11. dsPIC microcontroller readout stages.

The readout operation has two main stages, acquisition, and processing. The acquisition block samples the analog signals using the internal ADC continuously triggered by a Pulse Width Modulation (PWM) signal. The processing consists of simple data filtering using a Moving Average Filter (MAF). The procedure of a single readout resumes on three operations:

- ADC samples and stores the ten analog channels.
- Direct Memory Access (DMA) triggers and transfers the data to a Samples Buffer.
- The CPU does the arithmetic operations of the MAF and places it in a Collect buffer.

The PWM controls the S&H of the ADC, where its frequency will correspond to the acquisition sampling rate. Additionally, it has the option to phase shift to guarantee the phase rotation according to the stimulation signal for maximizing the amplitude sampled, with 1° resolution.

The processing stage employs an oversampling and averaging method to increase the output estimate resolution and Signal-to-Noise Ratio (SNR). Considering using a f_m equal to 1 kHz to detect structures as small as 0.26 mm at a recoater speed of 250 mm/s, the sampling frequency required is 31.25 kHz, the closest suitable for the SDS operation, allowing to gain two extra bits. The resulting filter accumulates 16 samples, yielding a cutoff frequency at 866 Hz. Considering the oversample and average (decimate), the throughput is lowered to 2 kHz, since f_s is reduced by OSR.

E. Firmware – Data Interface

The data interface connects the four high-speed dsPIC microcontrollers to the ESP32-S3 through SPI. Fig. 12 illustrates the design to perform such an operation.

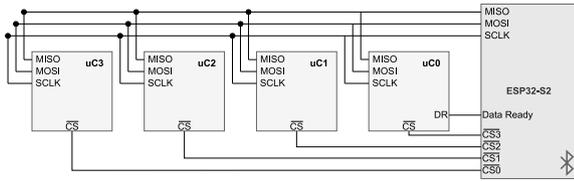


Fig. 12. SPI bus configuration for ESP32-S3 data interface.

The configuration chosen is standard, commonly known as cascade mode. The communication bus is shared among all the microcontrollers and has individual Chip Select (CS) for independent access. An integral aspect of the slave firmware development is the data-ready pin. The full-duplex SPI transmission uses two DMA channels. However, since the data readout uses another channel, the operations could not overlap, or one of the operations would be affected. The approach provides a data-ready signal that triggers at the end of each acquisition, making both processes possible to co-exist. This signal has 1.5625 kHz frequency to align with the data throughput after decimation. Considering a 250 mm/s recoater speed and the readout frequency established, the scan resolution would be at 0.16 mm (250 mm/1.5625 kHz).

However, due to the latency in the ESP32-S3 within the process of attending to the data-ready trigger, performing the SPI transfer, and asserting the necessary variables, the newer trigger could not be attended in time. This bottleneck led to performing a conservative access, as illustrated in Fig. 13.

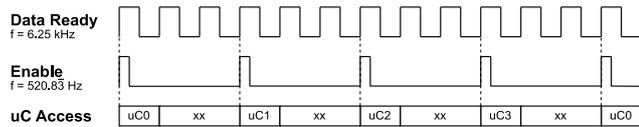


Fig. 13. Generic time diagram of ESP32-S3 data transfer.

The data transfer occurs every three cycles of the data-ready signal, meaning the resolution is lower. Considering the same recoater speed target and the 520.83 Hz readout frequency, the scan resolution stands at 0.48 mm (250 mm/520.83 Hz), translating to half the spatial resolution.

F. Firmware – Wireless Interface

The Wireless interface fully uses the ESP32-S3 capabilities to achieve such an anticipated goal. Firmware development was one of the most challenging parts of the WECAP, but it was simplified using the Espressif Software Development Kit (SDK). The architecture uses the FreeRTOS operating system kernel to manage concurrent threads integral to the system's operation.

The solution begins by defining the devices' role to function as a peripheral within the network, utilizing the Generic Access Profile (GAP) capabilities. Subsequently, the device effectively simulates two distinct communication channels as serial communication: one for writing data and another for reading. This emulation is achieved by establishing two crucial characteristics within the Generic Attribute (GATT) services table, namely the Receiver (RX) and Transmitter (TX). On top of this, the solution incorporates a third-party Python library on the computer side. This library facilitates selecting specific characteristics and maps them onto the appropriate COM Port channel.

The second development phase centered on integrating the SPI master, which orchestrates the transmission of commands

received from the host and the collection of scan data. Given BLEs' inherent low data throughput, a micro-SD card serves as a buffer for acquired samples.

III. ADVANCED EDDY CURRENT ARRAY PROBE

The StrixVision, is a complete ECP array aiming to enter the AM industry to QC PBF process parameters layer-by-layer. The design, illustrated in Fig. 14, uses an eight-PCB stackup, to guarantee a small form factor.

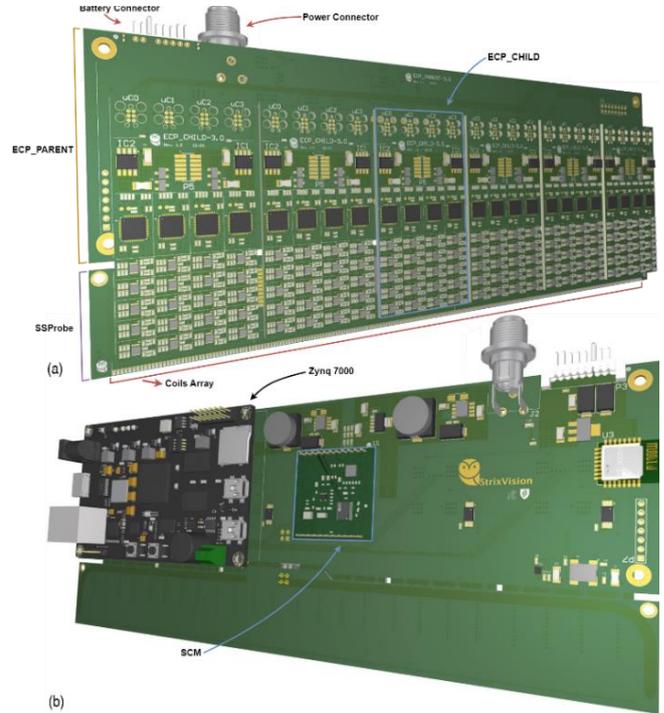


Fig. 14. StrixVision PCB front view (a) and back view (b).

The hardware separation between the three distinct PCB designs follows the WECAP concept. The architecture allows the different PCBs to be replaced independently without requiring a complete redesign. Most important is the ability to switch between different stimulation and sensing electromagnetic geometries to improve the results depending on the specimens in production.

Concerning the PCBs, the SSProbe integrates the stimulation coil and the sensing coils spaced by 1 mm. The ECP_Childs, referred to as Array Segment Cluster, have all the necessary readout hardware. Meanwhile, the ECP_Parent is responsible for power management and connecting all the PCBs. The connections are made through low-profile connectors to reduce the overall height, resulting in a compact design.

A. System Architecture

The system is an upgraded and more powerful version of WECAP, improving the less optimal characteristics while enhancing the scan length and the resolution capabilities. The architecture of the system is presented in Fig. 15.

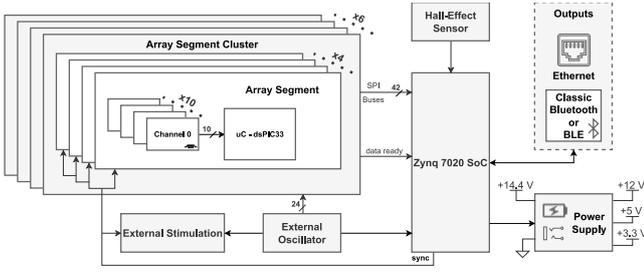


Fig. 15. StrixVision block diagram.

The developed architecture grows on top of the previous version core, with the main difference residing in scaling up the number of Array Segments from 4 to 24, with several stacked side by side. The electromagnetic geometry between stimulation and sensing is very similar, with upgrades only on the PCB design. The core component of WECAP, the dedicated SCM, remained unchanged due to its decent performance in driving independent stimulation coils, particularly with the resonant capacitor, enabling compatibility with a wide range of coils. The AFE, on the other hand, suffered upgrades to solve the previous limitations.

Currently, the device design supports 240 sensing coils, requiring 24 dsPIC microcontrollers for sampling, leading to a massive data amount with considerably high throughput. To keep up with the massive processing demand, StrixVision uses an Zynq 7000 System on Chip (SoC) to retrieve the six Array Segment Cluster data in parallel. The device operates in wireless mode using a 9800 mAh battery with a data interface through Bluetooth or cable mode with mains power and ethernet output. The specifications of the system are listed in Table II.

TABLE II. WECAP OVERALL SPECIFICATIONS

Dimensions	250x97 mm
Spatial Resolution (Coils pitch)	1 mm
Scan length	240 mm
Scan resolution (250 mm/s)	0.16 mm
Sampling rate	31.25 kHz
Readout Frequency	1.5625 ksp/s
Stimulation frequency	1 MHz
Array Segment clock	180 MHz
Interface clock	666 MHz
Supply Voltage	10 V
Power Consumption	12.89 W

B. Improved Probe Readout

The current AFE, like its predecessor, connects the sensing coil to the microcontroller ADC channel input. This design uses an AC-coupled non-inverter amplifier topology, as illustrated in Fig. 16.

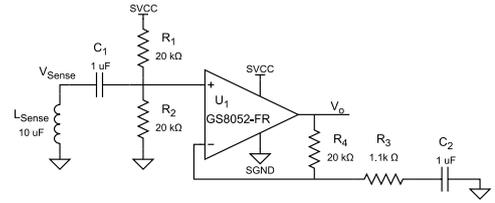


Fig. 16. Sense coil non-inverter amplifier schematic.

The topology operation is simple, starting by the coupling capacitor C_1 removing any DC voltage from the input signal. Subsequently, the resistive voltage divider created by R_1 and R_2 defines the voltage input to one-half of the power supply. The feedback capacitor, C_2 , prevents DC amplification, buffering it to the output through the feedback resistor. The feedback network defines the AC gain according to

$$V_o = \left(\frac{R_4}{R_3} + 1 \right) V_{sense} + \frac{SVCC}{2}. \quad (7)$$

The gain value employed is around 20, a value very much in line with its predecessor. This choice was validated as it effectively produces a signal close to the power supply rails while having a powerful primary magnetic field stimulation. Notably, C_1 and the parallel combination of R_1 and R_2 form an HPF tuned to 16 Hz, ensuring a flat frequency response around the stimulation frequency.

The rationale behind adopting this new topology arises from the limitations the previous approach had. Most notably, the input impedance is ten times higher, attenuating the loading effect on the source signal to acceptable levels. Furthermore, the topology separates the feedback network from the input, facilitating the maintenance of low resistor values for reduced noise. Additionally, this configuration eliminates phase inversion, simplifying the synchronization process. It is worth noting that the OPAMP is the same, with only the package being switched to a dual OPAMP option to reduce the overall footprint.

C. SoC Integration

The integration of Zynq-7000 into the system results from the demand for parallel processing to handle the amount of data generated by the array segment cluster, aiming to maintain the predecessor scanning resolution. The development process for the SoC includes two main components, the hardware description for the PL using VHDL and the firmware for the PS using C language. Fig. 17 illustrates the general functional blocks of the architecture.

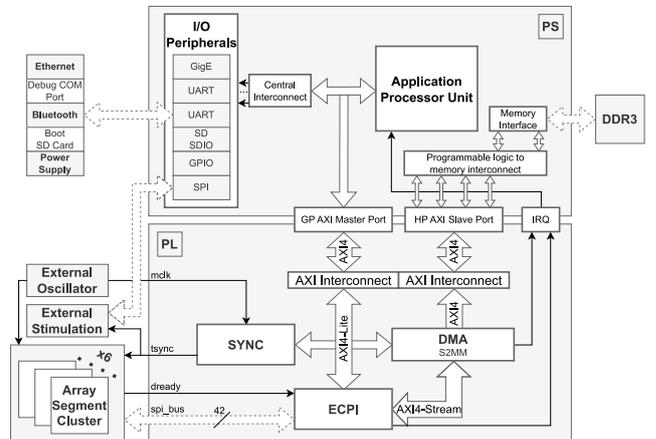


Fig. 17. Zynq-7000 SoC architecture block diagram.

The Xilinx native tools, the well-known Vivado 2022.2 and Xilinx Vitis 2022.2, allowed a very efficient development process. Vivado facilitated the design of Intellectual Property (IP) cores, including modules from scratch like Synchronism (SYNC) and Eddy Current Probes Interface (ECPI) and configuring pre-existing IPs such as DMA and the ARM cores. On the other hand, Xilinx Vitis supported the implementation of the firmware component, which is responsible for managing all the IP cores in use, the necessary PS peripherals, and the ethernet stack.

The system follows a bare-metal approach using a single core. It comprises four main processes: power management, digital synchronization, data acquisition and storage, and host interface. The PS and PL sides are actively responsible for performing these processes, with the PL responsible for the most demanding tasks. Communication between the PL and PS or between IP cores occurs through the standard Advanced eXtensible Interface 4 (AMBA AXI4) defined and controlled by Arm. This section provides detailed explanations of each process implementation.

D. Firmware – Digital Synchronization

Digital synchronization is mandatory considering the SDS concept, a feature already embedded in the WECAP version. Previously, the method relied on a master microcontroller within the array segment. However, the SoC offers a more accessible and flexible solution. The concept remains the same, it uses the shared oscillator signal (mclk) to generate a trigger for the DDS and the dsPIC microcontrollers to guarantee synchronization between the stimulation and the demodulation with a deterministic delay. Programming the DDS also shifted to the SoC Arm core responsibility.

E. Firmware – Data acquisition and storage

Data acquisition and storage are the core processes in the system and are the primary reasons for integrating the SoC. ECPI is the IP core designed to acquire the sensing data from all the microcontrollers. Additionally, it is responsible for handling the transmission of the configuration commands received from the host. Fig. 18 illustrates the ECPI functional blocks.

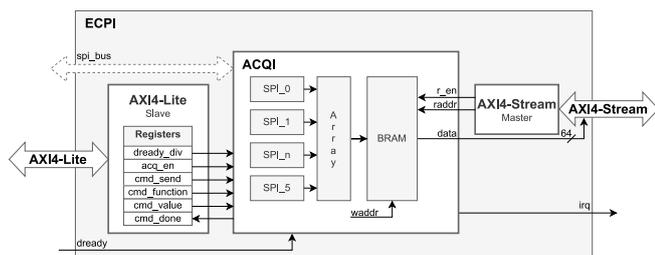


Fig. 18. ECPI architecture block diagram.

The PS side configures and controls the IP behavior through the AXI4-Lite slave interface. The AXI4-Stream interface is a high-performance streaming interface that allows faster transfer of the acquired data for storage in the DDR3. However, the primary operations occur under ACQUISITION Interface (ACQI), a wrapper to manage the master SPI cores with two internal state machines, one dedicated to sending commands and the other for retrieving the sensing data. The ECPI interfaces each array segment with a dedicated SPI bus with four microcontrollers.

It is important to emphasize that data transfer begins in synchronization with a data-ready signal provided by one of the microcontrollers. This approach, similar to the one used in

WECAP and represented in Fig. 19, ensures that the normal sampling process of the array segments microcontrollers is not disturbed.

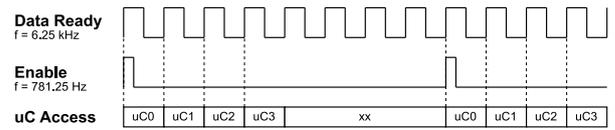


Fig. 19. Generic time diagram of ACQI data transfer.

In the diagram above, each data-ready rising edge triggers parallel data transfer from six microcontrollers, one of each array segment. This transfer occurs at a frequency of 781.85 Hz, changing according to the value set in the dready_div register following

$$f_{enable} = \frac{f_{data_ready}}{4 + dready_div} \quad (8)$$

As a result, the maximum enable-signal frequency achievable is 1.5625 kHz solving the WECAP latency issue. This frequency aligns with the 0.16 mm resolution goal for commercial PBF machines operating at 250 mm/s speed. It is important to emphasize that the sampling frequency within the array segment cluster is much higher, operating at 31.125 kHz.

F. Firmware – Host Interface

The host interface represents the communication between an external computer running the LabView application and the StrixVision. Depending on the operation mode, this interface can use Bluetooth or ethernet. In compliance with the development roadmap, the device only supports the ethernet interface.

The implementation relies on the most efficient approach, a bare-metal method using the Lightweight IP (LwIP), an open-source TCP/IP stack designed for embedded systems. It is suitable since it uses minimal resources while providing low latency and high throughput. The system behaves as a TCP server using a static IP address in the current configuration. In this design, the system waits for incoming TCP connections from the host to react accordingly.

IV. USER-INTERFACE

The user interface represents a sophisticated computer application developed using the LabVIEW Software capabilities, as shown in Fig. 20. This new application, developed from scratch, provides easy integration with several inspection systems.

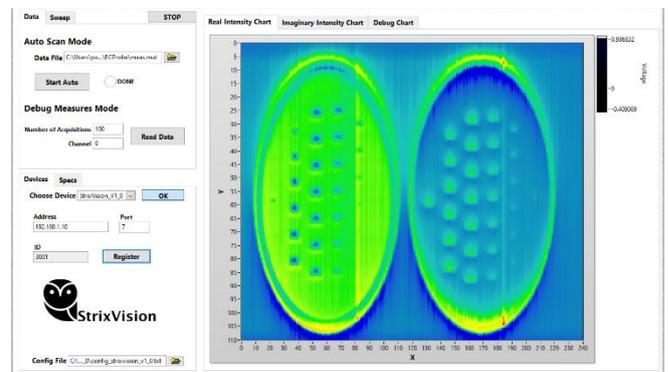


Fig. 20. GUI to control inspection probes and CNC.

The implementation uses a parent probe class with pre-defined empty functions (LabView VIs) such as initialization,

command transmission, data retrieval, and close. When installing a new device, the only requirement is to develop the drivers or even inherit some functions from other probes for simplification. Furthermore, some graphical tabs adjust dynamically based on the probe, facilitating the display of different connection types, configuration parameters, and calibration methods. The users only need to select the appropriate drivers during the operation.

The development process at first established a working version of WECA. The software development for StrixVision was minimal and straightforward. The existing skeleton provides everything, requiring only the development of drivers for the new communication layer.

The application also maintains the Computer Numerical Control (CNC) control capabilities since other inspection probes rely on it for achieving higher precision scans. This portion of the software has remained unchanged, except for its update into a class structure and enhancements to improve speed. It continues to support manual and automatic control of the probes' position.

V. RESULTS

Access to a real PBF machine is challenging, particularly in Portugal, where only a handful of companies might have. Negotiating an agreement to assemble the StrixVision on such expensive equipment is complex. Instead, the measurement setup, illustrated in Fig. 21, emulates the L-PBF setup.

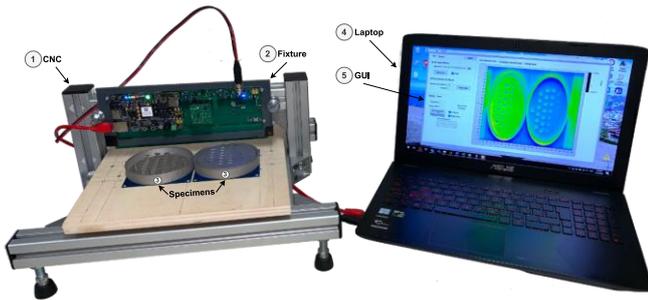


Fig. 21. StrixVision measurement setup.

The StrixVision mounts on a CNC (1) using a custom PVC fixture (2). The specimens (3) are placed on a wood base, enabling scan speeds up to 160 mm/min. The laptop (4), running the developed LabView application (5), handles the control, data acquisition, and the 2D image reconstruction.

A. Preliminary

After testing the equipment, the first step is to perform scans over 100x100 mm sample PCBs with distinct patterns. It is essential to assess what requires fine-tuning, such as stimulation current amplitude and MAF number of samples, and to verify the actual imaging reconstruction outcome. The PCBs' dark regions correspond to the Flame Retardant 4 (FR4) material and brighter areas to 0.35 μm copper.

The first scan is a simple circle pattern with an outer diameter of 25 mm and an inner of 15 mm (5 mm thickness), illustrated in Fig. 22 (a) with the amplitude imaging results in Fig. 22 (a) and (b).

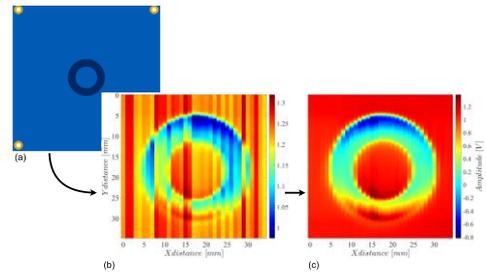


Fig. 22. Circle pattern (a), imaging result without compensation (b), and final imaging (c).

The imaging result in Fig. 22 (b) presents a significant mismatch among all the channels. The most evident reason is the channels' AFE differences, especially having 1% tolerance components defining the gain and the bias point, which could explain part of the problem. Second, the amplifier output impedance mismatches and the ADC sample and hold capacitor dispersion also contribute. However, the source is mainly from the coils' lift-off and orientation, which even with automated assembly is inevitable. Fortunately, there is a solution, and it is possible to improve the raw image and obtain the result in Fig. 22 (c). The method to enhance the data consists of performing a simple data processing under LabView before showing the final reconstruction, following

$$\text{result} = \frac{\text{rawscan} - c_{\text{air}}}{c_{\text{metal}} - c_{\text{air}}} \quad (9)$$

where rawscan is the scan measurement matrix, c_{air} , and c_{metal} are calibration measures obtained before initializing the scan with the probe placed on the air and over the metal, respectively. The Equation aims to compensate the rawscan measurements for sensitivity and offset mismatches. In the numerator, subtracting c_{air} from the rawscan allows removing the effects of lift-off. The division by $c_{\text{metal}} - c_{\text{air}}$ normalizes the data, ensuring the numerator falls into the expected range between metal and air, improving the sensitivity and the offset mismatches among all the channels.

B. PBF Specimens Imaging

The final validation test for StrixVisions' capabilities consists of one-layer imaging on two dimensional scans over LB-PBF-produced parts. These samples, manufactured using SS316 powder in a RenAM 500S Flex Laser Beam PBF (LB-PBF) machine present in Instituto de Soldadura e Qualidade (ISQ), were designed to emulate two variants of what an additive-manufactured part can be. Part one, illustrated in Fig. 23, is a high-density metal with negative structures, while part 2, in opposition, features positive metal structures depicted in Fig. 23 (b).

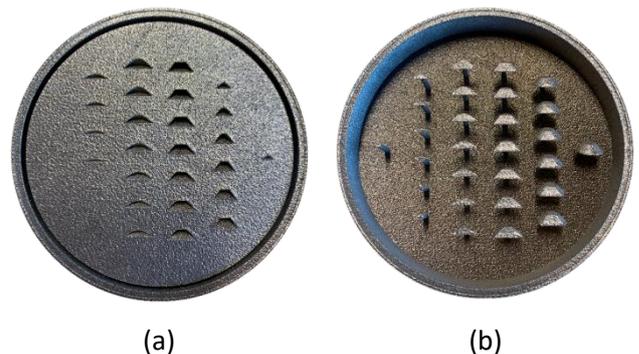


Fig. 23. Top view of the LB-PBF produced part 1 (a) and part 2 (b).

The specimens are designed with a frustum cone placed at different heights to create negative and positive structures. This design enables the evaluation of the probe with different superficial sizes and depths. The scanning area in the right image is an inversion of the negative part.

The probe setup includes a total lift-off of around 0.4 mm, with 0.3 mm attributed to the circular parts frame and 0.1 mm to prevent the probe from scratching the metal. In a real scenario, it would be reduced to 0.1 mm, providing higher sensitivity, but the probe still features a raw voltage variation between air and metal around 104 mV. The stimulation coil driving current is 700 mA peak to peak. The combined length of both parts side-by-side is 206 mm, requiring a single pass to obtain both results.

The imaging results for part one, in Fig. 24, accurately reconstruct the metal part, capturing variations in the superficial size corresponding to the structures. Additionally, it is possible to verify an apparent decrease in amplitude with the increase of the y-axis, which relates to the decrease in depth of the structures. Despite the channels mismatch over the metal, the variation in value is low compared to the structures' detection. Due to the decent SNR, the mismatch is neglectable in the reconstruction.

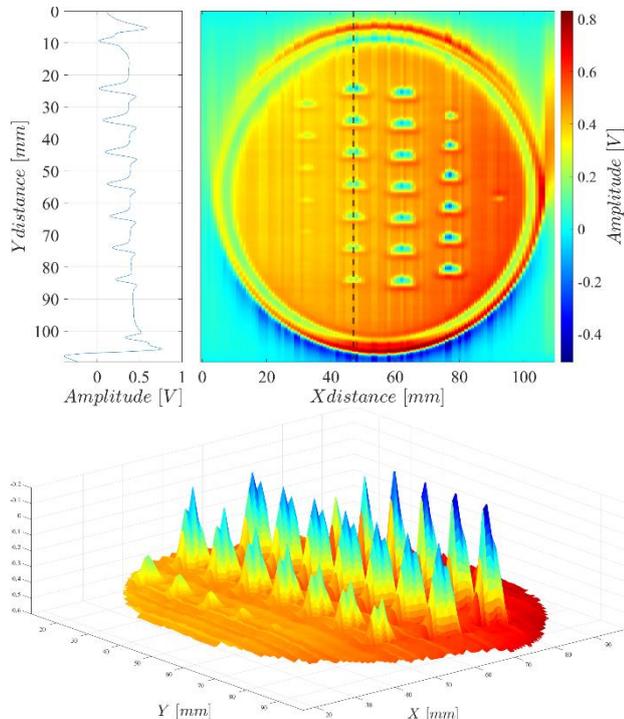


Fig. 24. Amplitude imaging result on a two-dimensional scan over the LB-PBF part 1.

The imaging result for metal part two, in Fig. 25 is decent, showing higher intensity in the superficial metal and a fadeout effect representing the depth of the structures. However, there is a decrease in sensitivity over the metal structures compared to the previous negative structures. A result from its inability to induce enough eddy current loops in small metallic structures. Negative structure detection is a different scenario because the eddy current loops have a wide metallic area to close, generating a strong secondary magnetic field.

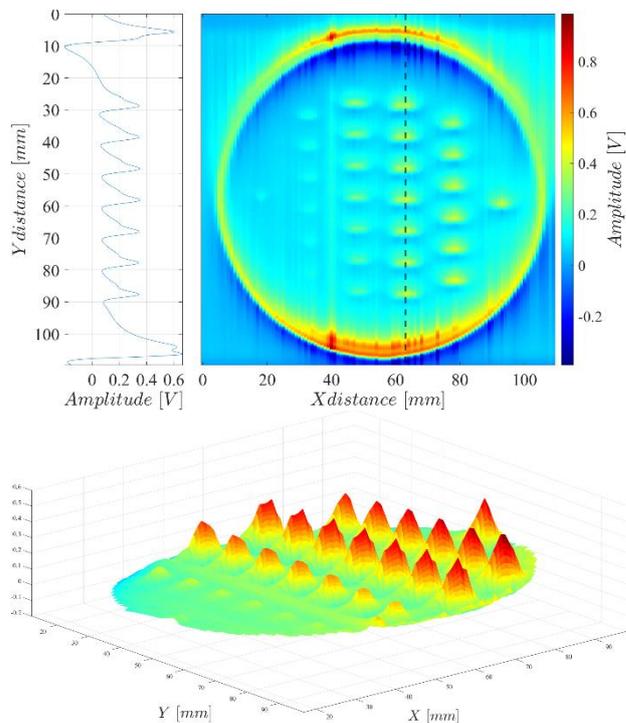


Fig. 25. Amplitude imaging result on a two-dimensional scan over the LB-PBF part 2.

The results above do not include the powder due to the post-cleaning process. However, the electrical conductivity of the powder is significantly lower than the consolidated material, not affecting the results [8]. In summary, the results align with the expectations for the StrixVision design. Retrieving data from the 240 channels in parallel with a 0.16 mm resolution along the y-axis is possible. However, the x-axis resolution must improve to characterize the smaller structures, either negative or positive.

VI. CONCLUSIONS

This work presents the development process of a new ECP array to scan PBF-produced parts layer-by-layer. Achieving the objectives demanded a deep dive into several domains, the electromagnetism fundamentals, and the architecture and design of a mixed signal embedded system.

WECAP emerged as a platform for studying, modeling, and validating the new concept. The probe successfully delivered a high-frequency readout with 0.48 mm scan resolution and a notable 1 mm spatial resolution. Moreover, the SCM provides a method to drive coils with a current achieving 700 mA peak-to-peak effectively and generate a strong magnetic field. The optimized probe, StrixVision, showcased remarkable progress, extending the scan length to 240 mm and reducing the scan resolution down to 0.16 mm. While successfully demonstrating imaging capabilities and PBF specimen reconstruction, some limitations in the resolution along the sensing line axis were noted.

Efforts are underway to validate the system's capabilities through upcoming tests on the RenAM 500S Flex LB-PBF machine at ISQ. These tests mark a crucial step towards addressing the existing limitations and advancing the technology. This work not only contributes significantly to the field but also opens avenues for future enhancements, ultimately shaping the future of AM.

This thesis ends up providing a complete ECP array device. Nonetheless, there is work remaining to fulfill the industry requirements. Below is listed the future work recognized as crucial:

- Continue the StrixVision missing features development: the wireless functionality and the position sensor (e.g., optical) to obtain the produced layers' start and finish positions.
- Validate the probes' layer-wise imaging performance in a real PBF machine.
- Improve the sensing and stimulation electromagnetic geometry. Improving the stimulation spatial resolution and attenuating the primary magnetic field baseline are vital for enhancing the imaging results.
- Study the possibility of using lower-size package coils or replacing the sensing sensors with MR to decrease the spatial resolution to better characterize the small structures on the specimens.

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