Ultra-Compact ΣΔ Modulator for Organ-on-Chip Systems

Fábio Miguel Magalhães Dias
Instituto Superior Técnico, Universidade de Lisboa, Portugal
fabio.dias@tecnico.ulisboa.pt

***Abstract*—This thesis presents the design of an ultra-compact Sigma-Delta (ΣΔ) modulator intended for integration into Organ-on-Chip systems, specifically addressing the third use case of the UNLOOC KDT project, which aims to sensorize a Skin-on-Chip setup. A quasi-passive 1st-order ΣΔ modulator topology is proposed for implementation, due to its miniaturization and power efficiency characteristics. The modulator is designed and fabricated using TSMC 65 nm technology, achieving 7.7 bit of resolution and a 20.91 µW power consumption at a 15 MHz sampling rate with an oversampling ratio of 128. Subsequent improvements result in a resolution of 8.2 bit and a power consumption of 9.42 µW in post-layout simulations. The final chip dimensions are 29.9 µm by 35.6 µm, corresponding to a total area of 1068 µm^2, which represents the smallest area among state-of-the-art ΣΔ converters. The results contribute to the ongoing advancement of Analog-to-Digital converters for biomedical applications, underscoring the significance of optimized design methodologies.**

***Index Terms*—ΣΔ Modulator, Passive Integration, Low-Area, Low-Power, Organ-on-Chip**

I. Introduction

Introducing a pharmaceutical product into the market requires clinical testing and validation involving both in vitro and in vivo experimentation on animal models. However, the dependence on animal models in drug development is troubled by methodological limitations that contribute to drug failures. Additionally, ethical concerns surround the use of animals in testing procedures. Furthermore, there exists a notable bias in human testing, often neglecting certain demographic groups such as children, women, and individuals from diverse ethnic backgrounds. According to estimates, adverse drug reactions are responsible for approximately 197000 deaths annually within the European Union, incurring a societal cost of €79 B [1]. The emergence of the Organ-on-Chip (OoC) technology presents a promising alternative to animal testing, offering a means for safe testing and validation: An OoC system comprising a small plastic device featuring a 3D-microstructured channel network capable of simulating complete organs' mechanical and physiological responses.

Project UNLOOC - Unlocking the data content of Organ-on-Chips - aims to develop, optimize, and validate electronic-based tools to build OoC models to replace animal and in-human testing [2]. The validation process spans five distinct use cases (UCs), as illustrated in Fig. 1, conducted across ten European countries involving over 51 organizations. For the third UC or UC3, an OoC platform is designed to replicate human skin, facilitating the evaluation of transdermal drug delivery, skin penetration, absorbance, and toxicity in a validated setting. INESC-ID and INESC-MN contribute to UC3 by developing an application-specific integrated circuit (ASIC) to bias, integrate, and amplify the signals produced by the sensors very low. Integrating these sensors and their analog front-end is essential to achieve miniaturization and multiplexing capabilities for the proposed systems on a chip. This platform includes instrumentation for controlling thermal, fluidic, and optical elements and diverse sensor functions for precise monitoring. These elements operate at low frequencies due to their long time constant phenomena [3].

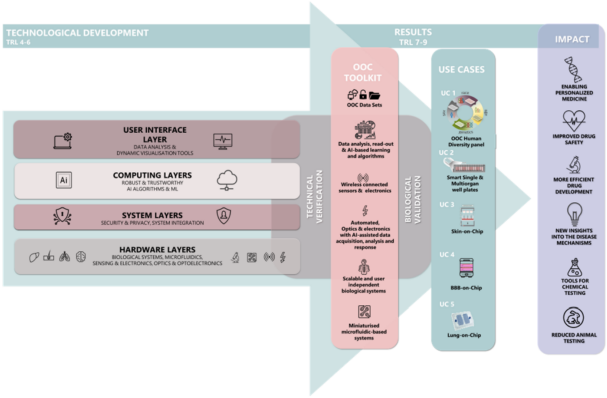


Fig. 1. UNLOOC Project Scope, Results, Outcomes, and Impacts [2].

Despite the analog nature of such phenomenons, the transmission, storage, and processing of information are usually performed in the digital domain, using either conventional digital computers or special-purpose digital signal processors [4]. Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are essential components in this context, bridging the two data forms.

Several architectures are used to implement ADCs, being the most relevant the Flash, the Successive Approximation Register (SAR), the Pipeline, and the Sigma-Delta (ΣΔ), each type having trade-offs between resolution, power consumption, area, sampling frequency, and the complexity of both analog and digital hardware. There is a specific interest in developing ADCs with low power consumption and minimal area for integration into large sensor matrix applications over their potential for integration with individual sensors [5]. Particularly, Sigma-Delta modulators (ΣΔMs) offer high resolution at relatively low signal bandwidths, making them particularly appealing for the UC3 due to their single serialized output

and miniaturization capabilities. This opportunity offers a promising step toward valuable advancements in both ADC and OoC technologies.

The proposed system for UC3 requires low power consumption to prevent overheating and maintain stable well temperatures, low noise levels to improve the limits of detectability, and support for interfaces with resistive, capacitive, and inductive sensors. As part of the UNLOOC project, the research presented in this document aims to develop a low-area ΣΔM. This ΣΔM is implemented in TSMC 65 nm technology [6], selected for its state-of-the-art capabilities and accessibility within INESC-ID's research group. Specific objectives have been identified to conduct the work:

- Area: Considering technology constraints and the expected sensor size estimated by the partner organizations, a target size of 50×50 µm is set, capable of supporting single-cell monitoring;
- Bandwidth: Given the aforementioned low bandwidth requirements of such systems, an objective of 50 kHz is established;
- Resolution: A resolution of 10 bit is considered suitable for the intended application, balancing precision with overall circuit complexity and, therefore, power consumption and silicon area utilization;

II. Literature Review of ADCs

The various ADC topologies offer flexibility to meet desired performance specifications. This section presents Figures-of-Merit (FoMs) relevant to this work and offers an overview of compact state-of-the-art converters, detailing the reasoning for choosing a ΣΔ topology.

A. Figures-of-Merit

Various authors employ different methods to calculate FoMs, with the most widely used approaches outlined in (1) and (2), where P_w is the power consumption of the converter, f_B stands for bandwidth, SNDR being Signal-to-Noise-and-Distortion Ratio, and ENOB the effective number of bits, also known as resolution. These FoMs can be expressed in both linear and logarithmic forms [7].

$$\mathrm{FoM}_1 = \mathrm{SNDR} + 10\ \log_{10}\left(\frac{f_B}{P_w}\right)\ \ [\mathrm{dB}] \tag{1}$$

$$\mathrm{FoM}_2 = \frac{P_w}{2 \cdot f_B \cdot 2^{\mathrm{ENOB}}}\ \ [\mathrm{fJ/conv-step}] \tag{2}$$

Notably, FoM_1 emphasizes effective resolution, whereas FoM_2 emphasizes power consumption [8]. Therefore, the larger the FoM_1 value and the smaller the FoM_2 value, the more favorable the ADC is. In the context of this work, where area is a crucial metric, defined as A, an alternative FoM is used, as shown in (3) [9].

$$\mathrm{FoM}_3 = \frac{P_w \cdot A}{2 \cdot f_B \cdot 2^{\mathrm{ENOB}}}\ \ [\mathrm{fJ \cdot mm^2/conv-step}] \tag{3}$$

B. Topology Selection Criteria

The various ADC topologies present advantages and limitations across the different performance metrics, including resolution, bandwidth, and power consumption, to name a few. Fig. 2 visually represents the relationship between resolution, represented as ENOB, and bandwidth, highlighting the clustering of different ADC types within specific regions.

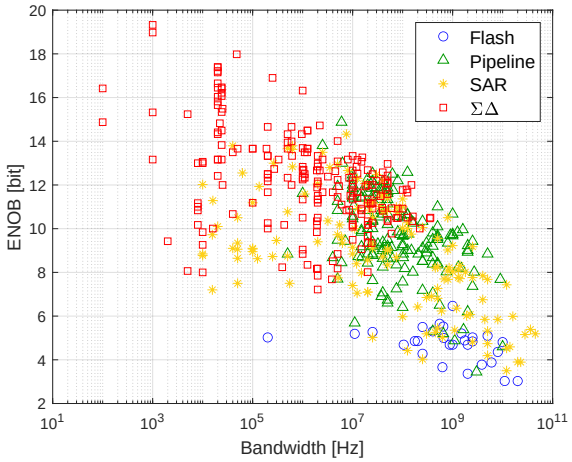


Fig. 2. Resolution vs. Bandwidth Analysis [10].

As shown in Fig. 2, ΣΔ ADCs provide the highest resolution for relatively low signal bandwidths. Nevertheless, different implementations have enabled their use in medium to high-frequency applications with reduced resolution. ΣΔ ADCs span a wide range of specifications, accommodating frequencies from 100 Hz to 360 MHz and an ENOB ranging from 7 to 20 bit. Conventional ADC types such as Flash, SAR, and Pipeline are preferred for high-speed applications, as they can handle signal bandwidths well above 1 MHz.

Multiple ΣΔ converters with ENOB exceeding 10 bit for the bandwidth of 50 kHz can be observed in Fig. 2. These results suggest that a converter with an ENOB of 10 bit, within the same bandwidth and using ΣΔ techniques, is expected to offer advantages in terms of area and power consumption. Thus, the ΣΔ ADC topology is considered most suitable for minimizing area and power requirements.

Further, a ΣΔ ADC or modulator can be selected. A modulator is sufficient because it provides a single serialized digital output, leading to a more compact design and lower power consumption. However, additional post-processing is necessary to achieve complete digitization, involving, for example, a field-programmable gate array to implement a decimator filter.

C. State of the Art in Compact ΣΔ ADCs

This subsection provides an overview of recent state-of-the-art ΣΔ ADCs, with a particular emphasis on integrated circuits (ICs) realized in nanometer-scale (smaller than 180 nm) technologies. The analysis is based on converters documented in the ADC survey by Boris Murmann, covering the period from 1997 to 2024 [10].

The present study aims to identify converters that minimize power consumption and chip area. A relationship between area and power is shown in Fig. 3. Among the circuits in the region below the gray dashed line, the six most recent are selected for further discussion. These six circuits exhibit high performance based on FoM_2 or FoM_3, or both, placing them in the top 5% of the analyzed devices [10].

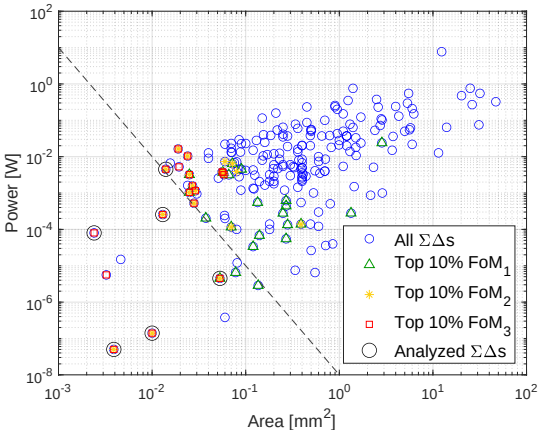


Fig. 3. Area vs. Power Consumption Analysis.

The analysis reveals that high resolution in ΣΔ converters requires amplification. This amplification often correlates to increased power consumption, particularly for systems with high bandwidth requirements. However, since power consumption is frequency dependent, achieving high resolution with low power consumption is possible if the bandwidth is sufficiently low. The absence of amplification and the reduced loop filter order enable compact implementations and decrease power consumption at the cost of lower resolution.

The circuit described by Gonçalo Rodrigues [11] is of particular interest for the present work as it is the smallest area ΣΔ converter identified. The circuit's performance metrics, summarized in Tab. I, reveal that the FoM_2 is inadequate, exceeding the acceptable threshold thereby indicating improvement potential. In contrast, the FoM_3 falls within adequate boundaries, suggesting that future studies should prioritize enhancements in power management. This ΣΔM also benefits from the continued availability of its original design team and files, having been proposed from within the INESC-ID research group in 2019. Accordingly, this circuit is selected for further development and adaptation to enhance its FoMs and meet the objectives previously specified while also contributing to the UNLOOC project [2].

III. The Quasi-Passive ΣΔ Modulator

A quasi-passive 1$^{\text{st}}$-order ΣΔM topology is selected for further development and study. This ΣΔM architecture exhibits low power consumption and occupies a minimal area due to the absence of operational amplifiers (OPAMPs). Consequently, the present work builds upon the existing design. This section describes the reference ΣΔM architecture, detailing its components, providing schematics, and explaining its operating principles.

TABLE I
Baseline ΣΔM Performance Metrics.

Technology [nm]	130
Supply Voltage [V]	1.2
Area [μm^2]	2400
Samp. Frequency [MHz]	100
Bandwidth [kHz]	390.63
ENOB [bit]	8.23
Power Consumption [μW]	80
FoM_2 [$\text{fJ/conv} - \text{step}$]	339.7
FoM_3 [$\text{fJ} \cdot \text{mm}^2/\text{conv} - \text{step}$]	0.82

A. Transfer Function

The conceptual block diagram of a ΣΔM, as shown in Fig. 4, is considered to derive the system's transfer function, which is essential for understanding its behavior. In this topology, the integration is done in the charge domain, using a transconductor-based front-end to convert the input voltage. Accordingly, obtaining the system's transfer function first requires an analysis of the integrator.

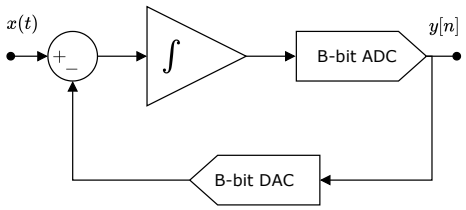


Fig. 4. Conceptual Diagram of a ΣΔM.

The simplified circuit of the switched-capacitor integrator is depicted in Fig. 5. This circuit operates in current mode by charging a sampling capacitor C_s, with a current proportional to the input voltage, resulting in a charge on C_s directly proportional to this input voltage. Subsequently, this charge is transferred to the integration capacitor C_i, where it is accumulated with the charges from prior samples. This accumulation produces an output voltage proportional to the input voltage's integral. Assuming the transconductance (g_m) cell is an ideal transconductor with transconductance G_m, V_{in} is a DC voltage because the sampling frequency f_s is significantly greater than the input bandwidth and δ is the duty cycle ratio of ϕ_1, the charge transferred during the sampling period can be expressed as in (4).

$$Q_s = \int_0^{\delta T_s} I\,dt = \int_0^{\delta T_s} (V_{in} \cdot G_m)\,dt = V_{in} \cdot \delta T_s \cdot G_m \quad (4)$$

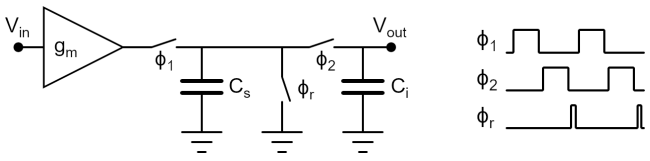


Fig. 5. Simplified Integrator Circuit and Respective Clock Phases.

Thus, the integration process begins by considering the charge equation in (4) during the period when ϕ_1 is active.

Additionally, the initial charge stored in C_i from the previous cycle is provided by (5).

$$Q_i[n-1] = V_{out}[n-1] \cdot C_i \tag{5}$$

Subsequencially, in the following integration phase, when ϕ_2 is active within the same clock period, the charge in C_s is transferred to C_i as expressed by (6).

$$Q_{out}[n] = Q_s[n] + Q_i[n-1] = V_{out}[n] \cdot (C_i + C_s) \tag{6}$$

Now, by replacing (4) and (5) into (6), (7) is achieved.

$$V_{out}[n] \cdot (C_i + C_s) = V_{in}[n] \cdot G_m \cdot \delta T_s + V_{out}[n-1] \cdot C_i \tag{7}$$

The conversion of (7) to the Z-domain yields (8) and (9).

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{\alpha}{1 - \beta z^{-1}} \tag{8}$$

$$\alpha = \frac{\delta T_s \cdot G_m}{C_s + C_i} \quad \wedge \quad \beta = \frac{C_i}{C_s + C_i} \tag{9}$$

The overall system transfer function can now be analyzed given (8) and (9). Fig. 6 shows the ΣΔM block diagram, which consists of an integrator with a feedback loop. Considering the output of the block diagram, $Y(z)$ represents the summing of $E(z)$, the quantization noise of an ideal quantizer, and the integrator output $I(z)$, as presented in (10).

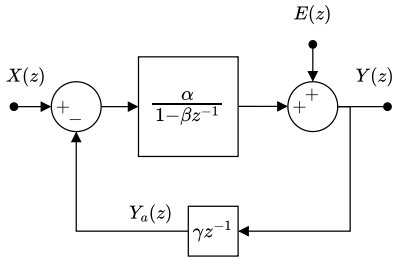


Fig. 6. Block Diagram of a 1st-order ΣΔM.

$$Y(z) = I(z) + E(z) \tag{10}$$

Further, it is important to note that $Y(z)$ undergoes digital-to-analog conversion within the feedback loop, resulting in an analog representation $Y_a(z)$ and that this process is controlled by a gain factor γ, which reflects its accuracy. Thus $I(z)$ can then be expressed in terms of $X(z)$, $Y(z)$, and $H(z)$ as:

$$I(z) = H(z)(X(z) - Y(z) \cdot \gamma z^{-1}) \tag{11}$$

By replacing the expression for $I(z)$ from (11) into (10) and simplifying, the overall transfer function of the system can be derived, resulting in:

$$Y(z) = X(z)\frac{H(z)}{1 + H(z) \cdot \gamma z^{-1}} + E(z)\frac{1}{1 + H(z) \cdot \gamma z^{-1}} \tag{12}$$

From here, two transfer functions can be derived: the signal transfer function (STF) and the noise transfer function (NTF). Replacing the expressions from (8) into (12) produces two transfer functions, (13) and (14).

$$\mathrm{STF}(z) = \frac{\alpha}{1 - (\alpha\gamma - \beta)z^{-1}} \tag{13}$$

$$\mathrm{NTF}(z) = \frac{1 - \beta z^{-1}}{1 - (\alpha\gamma - \beta)z^{-1}} \tag{14}$$

In the ideal case, $\gamma = \alpha = \beta = 1$, $\mathrm{STF}(z) = 1$ and $\mathrm{NTF}(z) = (1 - z^{-1})$, so the output consists of the input signal combined with the quantization noise, which is shaped by a first-order Z-domain differentiator or high-pass filter [4].

For the non-ideal case, the dependence of STF on α demonstrates that the input signal can be amplified without the requirement for OPAMPs [12]. Additionally, γ does not significantly affect the circuit, as long as $\alpha\gamma - \beta$ =0. Evaluating the condition where $\alpha\gamma$ is equal to β leads to (15).

$$\gamma = \frac{C_i}{\delta T_s \cdot G_m} \tag{15}$$

Although the actual value of γ is unknown, (15) identifies the value that results in optimal performance of the ΣΔM. From (9), it is known that β is always less than 1, causing charge loss and highlighting the need to control the ratio C_s/C_i when the capacitors are connected, as C_i must be significantly larger for C_s to be negligible and $\beta \approx$1. Also, C_s cannot be too small, as this would degrade system operation. Both these questions can be addressed by using a non-linear capacitor, implemented with recourse to a MOS capacitor (MOSCAP), which allows C_s to be larger during sampling while minimizing capacitance during integration [11].

B. ΣΔM Global Overview

The building blocks of the reference ΣΔM are examined to evaluate their contributions to the overall functionality of the system. The core elements of the system's architecture are: the g_m cell, the bootstrapped switch, the MOSCAPs, and the StrongARM comparator. A brief description of each component follows.

1) g_m cell: The g_m cell is a crucial component of the reference ΣΔM. As the front-end component of the circuit, it is the primary noise source. The implementation of the g_m cell employs an inverting amplifier [13]. The g_m cell continuously converts the input voltage to an output current, with a variable gain controlled by the dimensions of its constituent transistors and the number of cells used in parallel.

2) Bootstrapped Switch: Conventional switches, such as NMOS and PMOS transistors or transmission gates, exhibit an on-resistance that varies with input voltage. This dependence introduces distortion, particularly at nodes with significant voltage swings, making them unsuitable for all ADC nodes. The bootstrapped switches are applied to reduce distortion, stabilizing the gate-source voltage and minimizing on-resistance variation independent of the input voltage [14].

3) MOSCAPs: A MOSCAP comprises a MOS transistor with shorted source and drain terminals, functioning as a capacitor that stores charge between the gate and bulk terminals. The primary advantage of using MOSCAPs over traditional linear capacitors lies in their variable capacitance, which can be utilized to amplify signals and to reduce charge leakage [11, 15]. The chosen topology consists of two parallel complementary MOSCAPs [16]. Additionally, the ΣΔM comprises three sets of MOSCAPs: the sampling one, C_s; the feedback one, C_{DAC}; and the integrating MOSCAP, C_i.

4) Comparator: The StrongARM latch comparator is a commonly utilized topology characterized by low static power consumption, rail-to-rail outputs, and minimal input-referred offset [17]. The comparator consists of a clocked differential pair, and two cross-coupled pairs that form a latch, and four reset switches. When the reset signal is low, the outputs adjust based on the input voltage difference.

The top-level architecture of the quasi-passive ΣΔM is illustrated in Fig. 7. The MOSCAPs are depicted as variable capacitors. The bootstrapped switches correspond to switches S_1 to S_6, while switches S_7 to S_{12} are implemented as single transistor switches. The g_m cell and comparator are each represented using their respective symbols. The following section provides additional details and schematics for the discussed building blocks.

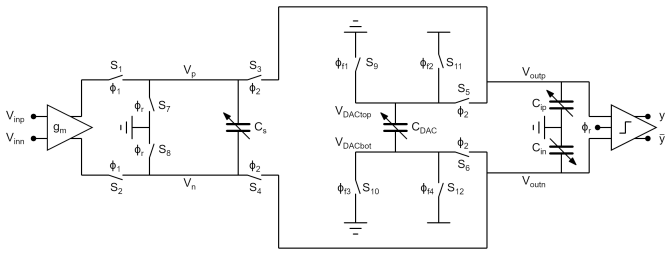


Fig. 7. Top-Level ΣΔM Circuit Schematic.

IV. ΣΔ Modulator Porting and Enhancement

The ΣΔM used as an initial reference for the proposed architecture lacks a complete layout but provides a floorplan that approximates the placement of its functional blocks, enabling area estimations. A tape-out run in TSMC 65 nm technology motivates the porting of the reference circuit and subsequent layout implementation for fabrication as an opportunity to verify the quasi-passive architecture in silicon and, thereby, add a practical component to the thesis. This work results in what is referred to as the first version of the ΣΔM from now on. Additionally, the development and optimization process of the first version quasi-passive ΣΔM is discussed, leading to a second and final version of the ΣΔM.

A. 1st ΣΔM Version

The primary objective of the first implementation is to achieve an operational design from which the layout can be developed to verify the quasi-passive ΣΔM architecture in silicon. The preliminary fabrication opportunity supports this development, although it imposes a tight tape-out schedule. Due to these time constraints, the porting process is conducted as directly and efficiently as possible, maintaining design dimensions and architecture where feasible. This subsection summarizes the process of porting the circuit from UMC 130 nm to TSMC 65 nm technology.

Many components used in the reference design are ideal blocks since it is not implemented in layout. These ideal blocks include the g_m cell resistors and the bootstrapped switch capacitor. Furthermore, the porting process requires replacing ideal blocks within the building block schematics. This procedure introduces the initial challenge of selecting suitable TSMC 65 nm technology capacitors and resistors. A study on MOSCAPs with an area of 1 μm^2 is also conducted. This study aids in understanding the differences associated with various MOSCAP sizing choices. Only transistors, capacitors, and resistances size adaptation is applied for these building blocks compared to the reference ΣΔM.

The comparator from the reference design exhibits limitations, particularly its lack of driving capability. A collaboration with João Silva from INESC-ID addresses these limitations by providing a more robust design incorporating inverter logic gates at the input clock and output nodes [18]. Fig. 8 shows the comparator, which includes one additional reset transistor and three inverter logic gates compared to the design used in the reference ΣΔM.

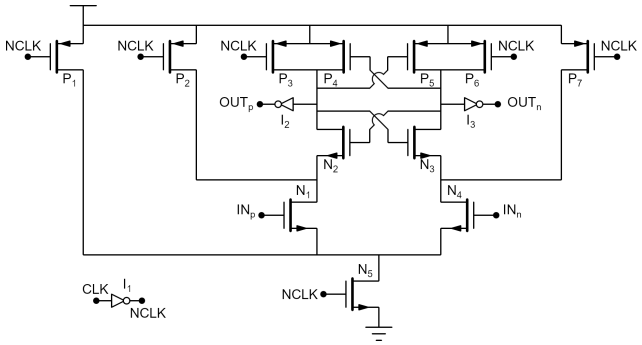
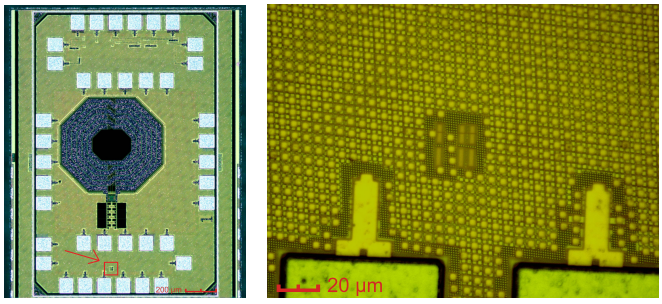


Fig. 8. 1st Version Comparator Circuit Schematic.

After porting, layout development and post-layout simulations lead to the fabrication of the first design. Fig. 9 shows two microscopic images of the fabricated IC die, captured at different zoom levels to highlight the various structures and features of the chip. In Fig. 9(a), the ΣΔM is highlighted in red, and it can be observed that the chip die is shared among multiple projects within INESC-ID. Fig. 9(b) provides a more detailed close-up, displaying elements such as capacitors, metal interconnects, and contact pads.



(a) Circuit Die (b) Close-up View

Fig. 9. Microscopic Images of the 1st Version ΣΔM.

The performance gains resulting from the changes presented in this section and the comparison between the post-layout simulation and the in-silicon results are detailed in Section V.

B. 2nd ΣΔM Version

The enhancement process begins with optimizing the simulation workflow of the ΣΔM. This optimization is necessary due to the inefficiencies of the existing process. It aims to ensure a smooth process in enhancing the circuit and enable additional validations on the ΣΔM design, such as Monte Carlo (MC) simulations. The improvements proceed with enhancements at the building block level, followed by the design and addition of clock generation.

One limitation of the initial g_m cell design is the excessive number of transistors in the signal path, which negatively impacts both dynamic range and noise performance. A modified design is proposed in which a clock signal regulates the gate voltage of the common-mode feedback PMOS transistors. This modification preserves the capability to switch the g_m cell on and off and improves dynamic range and noise performance while maintaining the same number of transistors and eliminating the switch transistors from the signal path. The implementation is illustrated in Fig. 10.

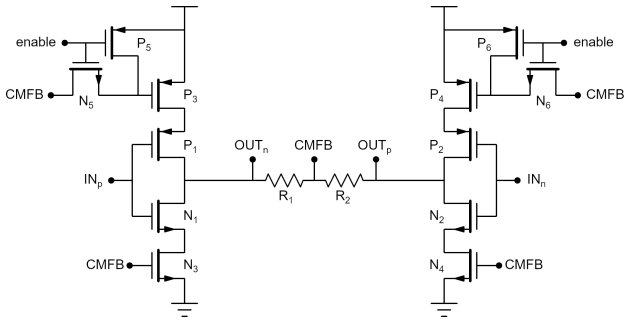


Fig. 10. Final g_m Cell Circuit Schematic.

The bootstrapped switch schematic, shown in Fig. 11, remains unchanged from the first version. Charge leakage is detected through the gate of switch N_3, which resultes in an overshoot at the output voltage during the transition to hold mode. This overshoot arises from charge transfer from C_b to the output load, which reduces the switch's ability to maintain the desired output voltage. Optimizations performed in Virtuoso ® ADE provide a sizing that minimizes charge leakage through the gate of N_3, achieving a reduction in C_b by a factor of three relative to the initial design.

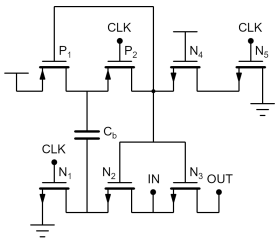


Fig. 11. Bootstrapped Switch Circuit Schematic.

In addition to the resizing associated with optimization, a modification is applied to the MOSCAP design to reduce area. For compactness, the number of parallel MOSCAPs, m, is set to 1 per MOSCAP in the final design, resulting in a higher aspect ratio, though it remains below 1.

Moreover, in the first circuit version, clock generation is provided externally, highly difficulting testing the system. A clock generation circuit is designed to meet to minimize the input signals on the IC and allow higher integration. The implementation utilizes a combination of logic gates from the TSMC tcbn65gplus standard cell library, which includes logic gates optimized with a small cell area. The design, simplified in Fig. 12, draws inspiration from traditional dual-modulus three-times dividers to generate three non-overlapping clocks [19]. Due to its feedback implementation, this design is free from bootup issues and is guaranteed to operate as expected after 3 clock cycles once powered. The complete circuit includes a total of 3 D-Flip-Flops, 3 NOTs, 2 NOR, 2 NAND, and an AND gate. Each component has different versions based on its driving capability, and, for every case, the lowest possible setting is chosen to reduce both power consumption and area usage. This circuit generates the required three non-overlapping clocks, ϕ_1, ϕ_2, and ϕ_r, as well as the enable signal, which controls the g_m cell. Fig. 13 illustrates a time diagram representing the behavior of these waveforms.

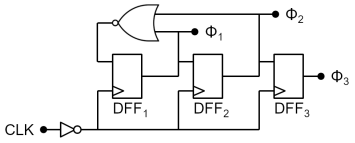


Fig. 12. Clock Generator Base Circuit Schematic.

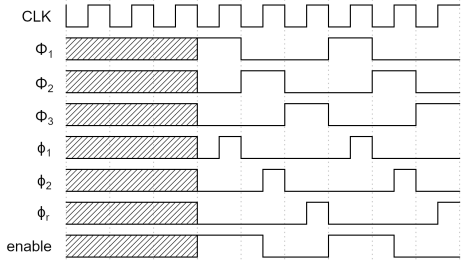


Fig. 13. ΣΔM Control Clocks Representation.

The design modifications presented thus far and subsequent layout optimization iterations result in the layout illustrated in Fig. 14, where the various components are labeled. The design successfully avoids performance bottlenecks, as later discussed, while ensuring compliance with the foundry's design rules. The dimensions of the layout are 29.9 µm by 35.6 µm, yielding a total active area of 1068 µm^2. A detailed breakdown of the area distribution is provided in Tab. II.

TABLE II
AREA DISTRIBUTION OF THE FINAL ΣΔM VERSION.

Building Block	**Area** [µm^2]	**Area Percentage** [%]
g_m Cell	82.6	7.7
MOSCAPs	580.0	54.3
Switches	158.6	14.9
Comparator	72.1	6.8
Control Logic	16.3	1.5
Clock Generator	42.7	4.0

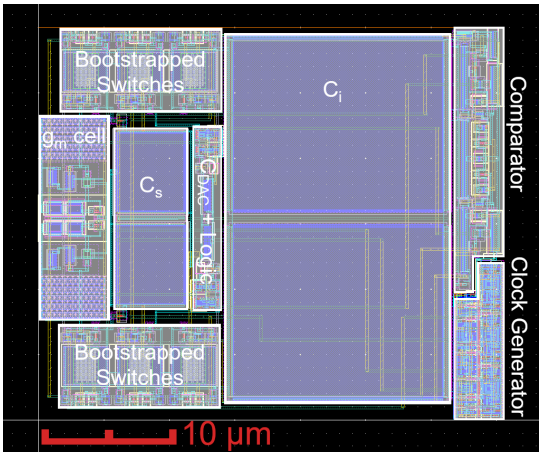


Fig. 14. Final ΣΔM Version Layout Implementation.

V. Results

The circuit test bench includes a differential input signal with an amplitude of 200 mV at a frequency of 20141.6 Hz, chosen to enable coherent sampling, and a sampling frequency of 15 MHz. A sinusoidal signal is combined with a DC voltage, set to 600 mV (half of the supply voltage, 1.2 V), to provide proper biasing for the g_m cell. The output voltage node y of the ΣΔM is analyzed to evaluate resolution by calculating the waveform's discrete Fourier transform (DFT), using 8192 points to ensure coherent sampling. Performance metrics, including ENOB and power consumption, are evaluated for each version discussed through simulations or experimental measurements for the in-silicon implementation.

A. 1st ΣΔM Version Simulation

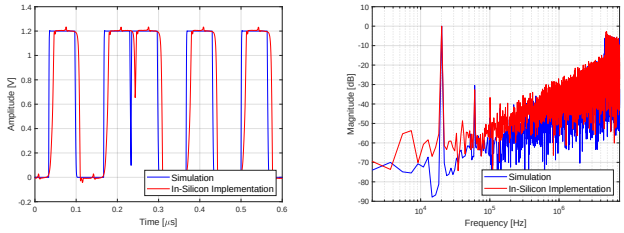
For the ΣΔM simulation test bench, an ideal output capacitor of 100 fF is used to simulate the input capacitance of a future decimator and evaluate whether the StrongARM comparator can drive such load. The output y is a binary waveform with a frequency of 15 MHz, modulated by the input differential voltage. The ENOB obtained for the post-layout first ΣΔM version with pads, assuming an oversampling ratio (OSR) of 128, is 7.68 bit. In contrast, with an OSR of 64, a particularly high third harmonic is not filtered, resulting in an ENOB of 4.52 bit, which is considered suboptimal. This inefficiency in resolution arises from saturation in the g_m cell, which induces aliasing. The second ΣΔM version addresses this problem. Furthermore, the analysis proceeds to power consumption, with the total power consumption of this implementation measuring 20.91 µW. This value is twice that of the pad-less version, primarily due to the biasing of the pads' electrostatic discharge protection circuit.

B. 1st ΣΔM Version In-Silicon Testing

Testing the in-silicon implementation presents several challenges. The fabricated chips are first encapsulated and wired prior to testing. Subsequently, to enable testing without the delay of manufacturing a custom printed circuit board (PCB), and considering that the tape-out of the circuit aims to validate simulations and the proposed architecture, the chips are evaluated using a Digilent ® Analog Discovery 2. This device is a compact and cost-effective USB oscilloscope operated through the free Digilent WaveForms software [20].

Fig. 15(a) displays the waveform comparison between the simulated and measured results for an example case. The signals exhibit similar characteristics, with the main distinction being the output load, which is higher for the in-silicon ΣΔM, resulting in increased rise and fall times. Additionally, the silicon implementation displays unexpected behavior, such as voltage spikes occurring in the middle of each bit value. This behavior is attributed to charge leakage due to parasitic capacitances. Fig. 15(b) illustrates the comparison between the simulated DFT and the measured data average DFT. The measured DFT reveals second-order effects, primarily due to layout asymmetries and the varying sizes of bonding wires, which influence the system's differential balance [21].

The measured ENOB values range from 4.56 bit to 7.31 bit, averaging 5.73 bit. As per power consumption, the measured value is 5.46 µW.

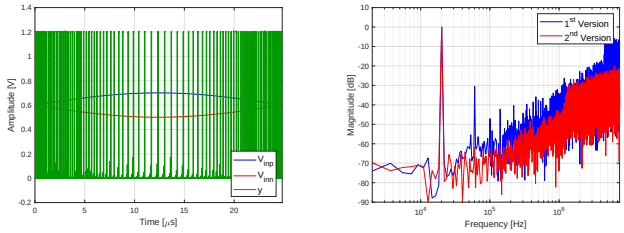


(a) Output Signals Example (b) DFT Comparison

Fig. 15. Comparison Between Simulation and In-Silicon Measurements.

C. 2nd ΣΔM Version Simulation

The simulation test bench for this version is identical to the one used in the first ΣΔM version. Fig. 16 presents half a period of the input voltages to illustrate the modulation effect and the resulting output DFT for both the first and second ΣΔM versions. The input differential voltage modulates the output y, as depicted in Fig. 16(a). As shown in Fig. 16(b), distortion due to odd harmonics is minimal in this ΣΔM implementation. The ENOB calculated from the spectrum, with an OSR of 128 under typical conditions, is 9.01 bit.



(a) Input vs. Output Signals (b) Output Signals DFT

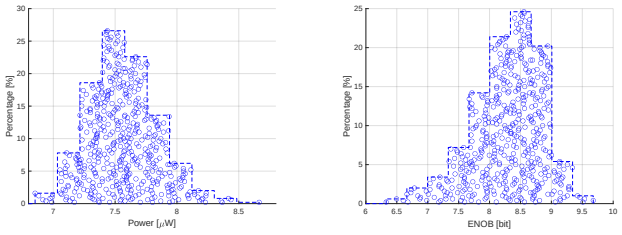
Fig. 16. Final ΣΔM Version Differential Transient Simulation.

In terms of energy, the total power consumption of this ΣΔM version measures 7.92 µW. Tab. III provides the power consumption for each building block, demonstrating that the g_m cell accounts for the largest portion at 35.7% of the total power. Furthermore, this ΣΔM version exhibits a balanced power distribution across the building blocks, with the three most demanding blocks having identical power consumption.

TABLE III
POWER DISTRIBUTION FOR THE FINAL VERSION ΣΔM.

Building Block	**Power** [µW]	**Power Percentage** [%]
g_m Cell	2.83	35.7
Bootstrapped Switches	0.17	2.2
StrongARM Comparator	2.45	30.9
Clock Generation and Logic	2.47	31.2

Moreover, corner simulations and MC simulations are conducted. The mean value of ENOB across all corner simulation cases is 8.19 bit, indicating a deviation of approximately 1 bit from the typical result. The fast-slow case exhibits the lowest resolution among the tested combinations, while the fast-fast combination achieves the highest resolution. Regarding power consumption, the fast-fast combination, referred to as the worst-power corner, demonstrates the highest power consumption, whereas the slow-slow combination results in the lowest. As expected, power consumption increases with rising temperature. MC simulations are performed using 500 points [22], accounting for variations in mismatch and process. The statistical distributions for power consumption and ENOB derived from the process-only simulations are presented in Fig. 17. The power distribution has a mean of 7.56 µW with a standard deviation of 0.27 µW, consistent with typical results. For ENOB, the mean is 8.29 bit with a deviation of 0.56 bit. The MC simulations for both mismatch and process variations yield similar results, indicating that neither significantly impacts performance.



(a) Power Consumption (b) ENOB

Fig. 17. Statistical Distributions from the MC Simulations.

Post-layout simulations are also conducted to verify that the introduced parasitics do not significantly affect performance. The layout in Fig. 14, without circuit pads, achieves an ENOB of 8.2 bit. Power consumption increases by 1.5 µW, resulting in 9.42 µW under typical conditions. The inclusion of circuit pads does not substantially affect the resolution, leading to an ENOB of 7.9, while power consumption increases to 10.2 µW. The limited impact of layout parasitics on performance is due to careful layout optimization, which incorporates insights from the various design processes.

Lastly, a standard analysis is presented in Fig. 18, illustrating the relationship between SNDR and input amplitude. The peak SNDR values recorded are 67 dB and 64 dB for the second ΣΔM version under typical conditions pre- and post-layout simulations, respectively. These values are obtained for an input differential amplitude of -2.5 dBFS or 225 mV.

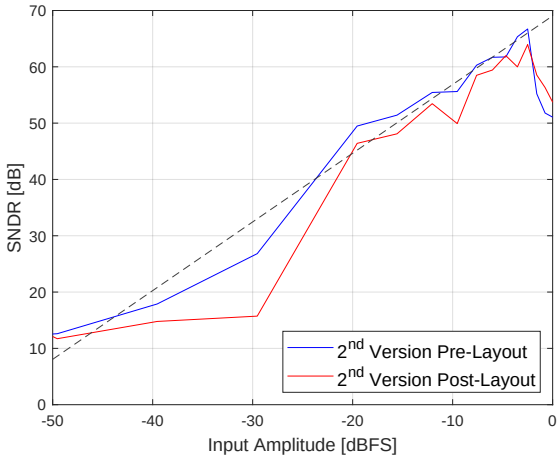


Fig. 18. Measured SNDR vs. Input Amplitude Analysis.

D. Discussion

The obtained ENOB for the presented implementations closely aligns with the original result of 8.23 bit, presented in Tab. I. In terms of power consumption, the first ΣΔM version exhibits a reduction of 3.8 times compared to the original results. The g_m cell is the primary contributor, accounting for 64.5% of total power, followed by the comparator. This comparator implementation, however, achieves a 25% improvement in power efficiency while providing sufficient load capacity relative to the original comparator version.

The results from simulations and measurements of the first ΣΔ implementation are summarized in Tab. IV. Despite being within the same order of magnitude, a more precise calculation method could further enhance alignment between the results. The differences highlight the importance of revising the testing procedure for future tape-outs. A custom PCB is anticipated to yield results that better align with simulations. Bonding imperfections may still occur even with microscopic verification, suggesting that circuits with significantly reduced resolution may have connection issues. Nonetheless, the variations between the simulations and the taped-out circuit remain within an acceptable range, validating the functional aspect of the ΣΔM architecture.

TABLE IV
PERFORMANCE METRICS COMPARISON BETWEEN SIMULATION AND IN-SILICON MEASUREMENTS.

Tested Metric	**Simulation**	**In-silicon Measurements**		
		Min.	**Avg.**	**Max.**
ENOB [bit]	7.68	4.56	5.73	7.31
Power Consumption [µW]	10.09	-	5.46	-

Following, the second ΣΔM version demonstrates a reduction in power consumption by a factor of 10 compared to the values presented by the reference ΣΔM and a 32% reduction from the first implementation while generating the necessary control clocks and exhibiting increased complexity. For instance, the individual power consumption of the g_m cell shows a reduction by a factor of 2.5 compared to the first implementation, which supports the improvements in the new design. In addition to the increased complexity and enhanced resolution under typical conditions, the final version exhibits a reduction of 2.3 times in terms of area compared to the reference design.

The performance of all modulator versions discussed in this document is compared with those presented in Section II-C. The relationship between area and power, illustrated in Fig. 19, indicates that the final ΣΔM is the smallest ΣΔ converter among the surveyed circuits [10].

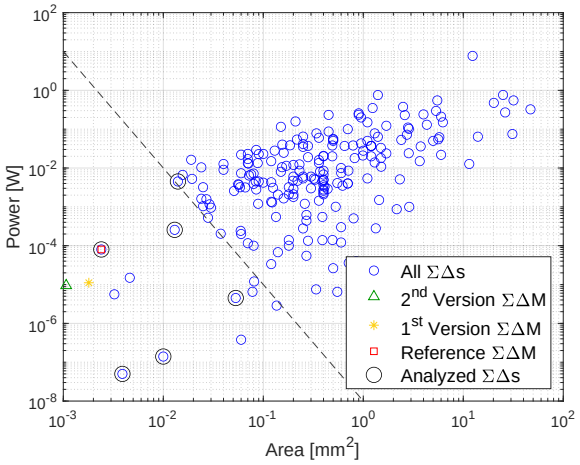
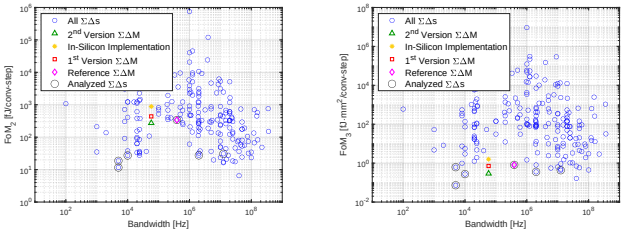


Fig. 19. Area vs. Power Consumption Analysis.

Next, the FoM_2 and FoM_3 values are calculated, yielding 273.4 fJ/conv-step and 0.292 fF·mm^2/conv-step, respectively. These results, depicted in Fig. 20, indicate an improvement of 20% in FoM_2, while FoM_3 shows a reduction by a factor of 2.8. Although FoM_2 is reduced compared to the reference ΣΔM, it remains above the acceptable 20 fJ/conv-step value. For FoM_2 to fall within an acceptable range, it must be further reduced by a factor of 14. This reduction can be achieved through enhancements in resolution, power consumption, and adjustments to sampling frequency. Attaining a satisfactory FoM_2 appears feasible with the proposed design, although it requires significant time investment. Nevertheless, the work presented in this document emphasizes minimizing area, which is accomplished, thereby addressing the gap in ΣΔ converters for the bandwidth range of 25 kHz to 350 kHz, ensuring a competitive FoM_3 within this range.

At last, the performance metrics are summarized in Tab. V. This section concludes the thesis work, with the contributions and potential future research directions outlined in the following section.



(a) FoM_2 (b) FoM_3

Fig. 20. FoMs vs. Bandwidth Analysis.

TABLE V
FINAL ΣΔM PERFORMANCE METRICS.

Technology [nm]	65
Area [μm^2]	1068
Supply Voltage [V]	1.2
Samp. Frequency [MHz]	15
Bandwidth [kHz]	58.59
ENOB [bit]	8.2
Power Consumption [μW]	9.42
FoM_2 [fJ/conv − step]	273.35
FoM_3 [fJ · mm^2/conv − step]	0.29

VI. CONCLUSION

To summarize, in this thesis, a low-area, low-power ΣΔM, designed for integration into OoC systems with a specific focus on UC3 of the UNLOOC project, is successfully developed, taped-out, tested, and optimized using the 65 nm TSMC technology. The following points summarize the most significant achievements throughout the project:

- Chip Manufacturing: Familiarity with the tape-out procedure is developed, encompassing the preparation and submission process required to manufacture the IC. This development facilitates a smoother transition from design to silicon implementation in the final ΣΔM design.
- Design Validation: The original modulator topology undergoes validation by testing the manufactured circuit. This validation confirms that the design meets the expected resolution and power consumption.
- Workflow Improvement: Significant simulation workflow improvements occur. By optimizing this process, it becomes possible to conduct MC simulations with the required number of points and to include parasitic simulations that would otherwise take months to perform.
- Compact Area: The final design achieves a notable reduction in area, measuring 1068 μm^2, which is 2.3 times smaller than the original version. The developed ΣΔM is the smallest ΣΔ converter among the surveyed circuits, reinforcing its suitability for miniaturized applications. The square geometry also provides advantages as it is compatible with large sensor matrices.
- Adequate Resolution: The final version of the modulator achieved an ENOB of 8.2 bit, with minimal resolution degradation attributed to parasitic effects from the layout.

- Power Efficiency: The modulator demonstrates a low power consumption of 9.42 µW, which is suitable for the power-constrained environment of OoC applications. This represents an improvement of 8.5 times compared to the reference ΣΔM, ensuring reliable operation without introducing thermal stress.
- Target Bandwidth: The bandwidth achieved meets the target of 50 kHz, making the modulator suitable for the real-time monitoring required by the UNLOOC project.

In terms of future work, the first objective is to increase ENOB to exceed 10 bits. Achieving this requires an OSR greater than 151 using the proposed architecture. Further optimization can be accomplished by refining the circuit layout and addressing parasitic effects through techniques such as the use of dummy transistors or modifications to the front-end architecture, with particular emphasis on the g_m cell. Moreover, enhancement of the FoM_2 is identified as another area of improvement. Next, the final ΣΔM design already occupies a significantly smaller area than other ADCs. One method to further reduce the area is to adopt more advanced CMOS processes with smaller transistor dimensions. Since the employed topology does not utilize amplifiers, the impact of short-channel effects is expected to be negligible. Finally, the fabrication of the developed circuit is necessary to validate its performance and identify design issues related to temperature dissipation, which are critical to its intended application. Due to the time constraints of a master's thesis, fabricating and testing multiple circuits is not feasible, as this process typically takes several months. However, the final ΣΔM is prepared for fabrication, which is expected to occur during the tape-out run in December 2024. Incorporating testability features in the design would facilitate more efficient debugging and provide a better understanding of discrepancies between experimental and simulation results. A custom PCB must also be designed to test the ΣΔMs effectively.

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