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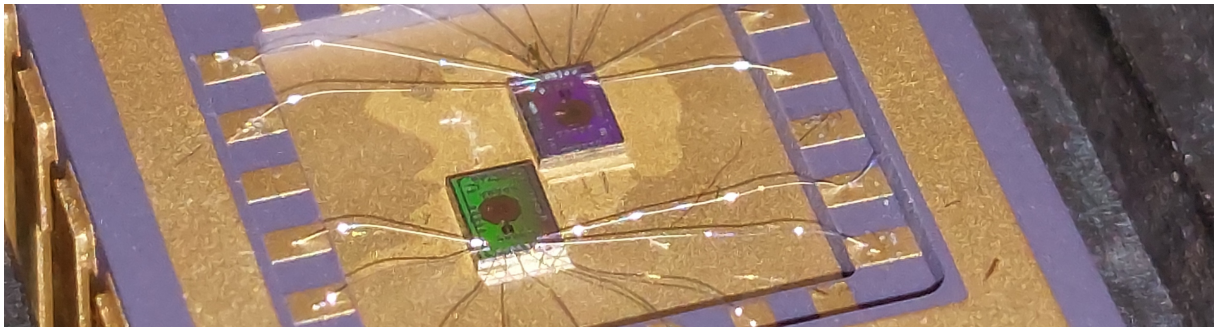

Ultra-Compact ΣΔ Modulator for Organ-on-Chip Systems

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Thesis to obtain the Master of Science Degree in

Electrical and Computer Engineering

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Declaration

I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

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The completion of this thesis represents the culmination of over two years of dedicated work, a milestone I could not have achieved without the support and guidance of many remarkable individuals. I would like to take this opportunity to express my gratitude to each of them.

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Finally, I thank any reader who takes the time to build upon this work. I am genuinely proud of what I have accomplished here, and it would mean the world to me if my research inspires future endeavors.

Resumo

Esta tese apresenta o design de um modulador Sigma-Delta ($\Sigma\Delta$) ultra-compacto, destinado à integração em sistemas de Órgãos-em-Chip, abordando especificamente o terceiro caso de estudo do projeto UNLOOC KDT, que visa a sensorização de um dispositivo de Pele-em-Chip. É proposta uma topologia quase-passiva de 1ª ordem para a implementação do modulador $\Sigma\Delta$, devido às suas características de miniaturização e eficiência energética. O modulador é projetado e fabricado utilizando a tecnologia de $65\,\mathrm{nm}$ da TSMC, alcançando $7.7\,\mathrm{bit}$ de resolução e $20.91\,\mu\mathrm{W}$ de consumo de potência a uma frequência de amostragem de $15\,\mathrm{MHz}$ com uma razão de sobreamostragem de 128. Melhorias adicionais resultam numa resolução de $8.2\,\mathrm{bit}$ e num consumo de potência de $9.42\,\mu\mathrm{W}$ em simulações pós-layout. As dimensões finais do chip são $29.9\,\mu\mathrm{m}$ por $35.6\,\mu\mathrm{m}$, correspondendo a uma área total de $1068\,\mu\mathrm{m}^2$, que representa a menor área entre os conversores $\Sigma\Delta$ do presente estado da arte. Os resultados contribuem para o atual avanço de conversores analógico-digitais para aplicações biomédicas, sublinhando a importância de metodologias de design otimizadas.

Palavras Chave

Modulador $\Sigma\Delta$, Integração Passiva, Área Reduzida, Baixo Consumo, Órgãos-em-Chip

Abstract

This thesis presents the design of an ultra-compact Sigma-Delta ($\Sigma\Delta$) modulator intended for integration into Organ-on-Chip systems, specifically addressing the third use case of the UNLOOC KDT project, which aims to sensorize a Skin-on-Chip setup. A quasi-passive 1st-order $\Sigma\Delta$ modulator topology is proposed for implementation, due to its miniaturization and power efficiency characteristics. The modulator is designed and fabricated using TSMC $65\,\mathrm{nm}$ technology, achieving $7.7\,\mathrm{bit}$ of resolution and a $20.91\,\mu\mathrm{W}$ power consumption at a $15\,\mathrm{MHz}$ sampling rate with an oversampling ratio of 128. Subsequent improvements result in a resolution of $8.2\,\mathrm{bit}$ and a power consumption of $9.42\,\mu\mathrm{W}$ in post-layout simulations. The final chip dimensions are $29.9\,\mu\mathrm{m}$ by $35.6\,\mu\mathrm{m}$, corresponding to a total area of $1068\,\mu\mathrm{m}^2$, which represents the smallest area among state-of-the-art $\Sigma\Delta$ converters. The results contribute to the ongoing advancement of analog-to-digital converters for biomedical applications, underscoring the significance of optimized design methodologies.

Keywords

$\Sigma\Delta$ Modulator, Passive Integration, Low-Area, Low-Power, Organ-on-Chip

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List of Acronyms

g_m	Transconductance
$\Sigma\Delta$	Sigma-Delta
$\Sigma\Delta$**M**	Sigma-Delta Modulator
AAF	Anti-Aliasing Filter
ADC	Analog-to-Digital Converter
ADE	Analog Design Environment
ALC	Alternate Loading Capacitors
APS	Accelerated Parallel Simulator
ASIC	Application-Specific Integrated Circuit
C&H	Charge-and-Hold
CMFB	Common-Mode Feedback
CMOS	Complementary Metal-Oxide Semiconductor
CT	Continuous-Time
DAC	Digital-to-Analog Converter
DC	Direct Current
DFF	D-Flip-Flop
DFT	Discrete Fourier Transform
DNL	Differential Non-Linearity
DRC	Design Rule Check
DT	Discrete-Time
ENOB	Effective Number of Bits
ESD	Electrostatic Discharge
FoM	Figure-of-Merit
FPGA	Field-Programmable Gate Array
FS	Full-Scale
IC	Integrated Circuit
INL	Integral Non-Linearity
LP	Low-Pass
LPF	Low-Pass Filter
LVS	Layout vs. Schematic
MASH	Multi-Stage Noise Shaping
MC	Monte Carlo

MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOS	Metal-Oxide Semiconductor
MOSCAP	MOS Capacitor
NAND	Not AND
NMOS	N-type MOS
NOR	Not OR
NTF	Noise Transfer Function
OoC	Organ-on-Chip
OPAMP	Operational Amplifier
OSR	Oversampling Ratio
PCB	Printed Circuit Board
PEX	Parasitic Extraction
PMOS	P-type MOS
Poly	Polysilicon
PVT	Process, Voltage, and Temperature
RC	Resistor-Capacitor
RMS	Root Mean Square
RSS	Root Sum of Squares
S&H	Sample-and-Hold
SAR	Successive Approximation Register
SC	Switched Capacitor
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SSH	Secure Shell
STF	Signal Transfer Function
T&H	Track-and-Hold
THD	Total Harmonic Distortion
TIA	Transimpedance Amplifier
UC	Use Case
USB	Universal Serial Bus
WPE	Well Proximity Effect

List of Symbols

α_1	Active integrator gain coefficient	
α_2	Passive integrator gain coefficient	
α_3	Quasi-Passive integrator gain coefficient	
β_1	Active integrator leakage coefficient	
β_2	Passive integrator leakage coefficient	
β_3	Quasi-Passive integrator leakage coefficient	
γ	Digital-to-analog conversion gain coefficient	
δ	Duty cycle ratio of phase clock ϕ_1	
μ	Mobility of charge carriers in a transistor	$\mathrm{m}^2/\mathrm{V}\cdot\mathrm{s}$
A_0	Operational amplifier DC voltage gain	
C_i	Integrator capacitor of an integration circuit	F
C_{ox}	Gate oxide capacitance per unit area of a transistor	F/m^2
C_s	Sampling capacitor of a sampling circuit	F
ENOB	Effective Number of Bits	bit
f_B	Signal bandwidth	Hz
f_N	Nyquist frequency	Hz
f_s	Sampling frequency	Hz
FoM_1	Figure-of-Merit that emphasizes effective resolution	dB
FoM_2	Figure-of-Merit that emphasizes power consumption	$\mathrm{fJ/conv-step}$
FoM_3	Figure-of-Merit that emphasizes circuit area	$\mathrm{fJ}\cdot\mathrm{mm}^2/\mathrm{conv-step}$
G_m	Total transconductance of a circuit	S
$H_i(z)$	Generic Z-transform non-delaying transfer function of an integrator	
$H_{qp}(z)$	Z-transform transfer function of the quasi-passive integrator	
L	Length of a transistor	m
m	Number of transistors in parallel for a given device	
Q_x	Change stored in C_x	C
R_{eq}	Equivalent resistance of a switched capacitor circuit	Ω
R_{on}	Equivalent resistance of a transistor biased in the triode region	Ω
SNR	Signal-to-Noise Ratio	dB
SNDR	Signal-to-Noise-and-Distortion Ratio	dB
T_s	Sampling period	s

THD	Total Harmonic Distortion	dB
V_{th}	Threshold voltage of a transistor	V
V_1	Fundamental or first harmonic of a signal	V
V_i	i^{th}-order harmonic of a signal	V
V_n	Output noise of a signal	V
W	Width of a transistor	m
W/L	Aspect ratio of a transistor	
$X(f)$	Fourier transform of $x(t)$	
$x(t)$	Example band-limited signal	
$x[n]$	Sampled representation of $x(t)$	
$x_q[n]$	Quantized representation of $x[n]$	
$X_s(f)$	Fourier transform of $x(nT_s)$	
$X(z)$	Z-transform of $x[n]$	
$y[n]$	Resulting signal obtained by digitizing $x(t)$	

Chapter 1

Introduction

1.1 Motivation

Introducing a pharmaceutical product into the market requires clinical testing and validation involving both in vitro and in vivo experimentation on animal models. However, the dependence on animal models in drug development is troubled by methodological limitations that contribute to drug failures. Additionally, ethical concerns surround the use of animals in testing procedures. Furthermore, there exists a notable bias in human testing, often neglecting certain demographic groups such as children, women, and individuals from diverse ethnic backgrounds. According to estimates, adverse drug reactions are responsible for approximately 197000 deaths annually within the European Union, incurring a societal cost of €$79\,\mathrm{B}$ [1, 2]. The emergence of the Organ-on-Chip (OoC) technology presents a promising alternative to animal testing, offering a means for safe testing and validation: An OoC system comprising a small plastic device featuring a 3D-microstructured channel network capable of simulating complete organs' mechanical and physiological responses.

Project UNLOOC - Unlocking the data content of Organ-on-Chips - aims to develop, optimize, and validate electronic-based tools to build OoC models to replace animal and in-human testing [3]. The validation process spans five distinct use cases (UCs), as illustrated in Fig. 1.1, conducted across ten European countries involving over 51 organizations. For the third UC or UC3, an OoC platform is designed to replicate human skin, facilitating the evaluation of transdermal drug delivery, skin penetration, absorbance, and toxicity in a validated setting. INESC-ID and INESC-MN contribute to UC3 by developing an application-specific integrated circuit (ASIC) to bias, integrate, and amplify the signals produced by the sensors [4, 5]. Integrating these sensors and their analog front-end is essential to achieve the required miniaturization and multiplexing capabilities for the proposed systems on a chip. This platform includes instrumentation for controlling thermal, fluidic, and optical elements and a diverse array of sensor functions for precise monitoring. These elements operate at low frequencies due to their long time constant phenomena [6].

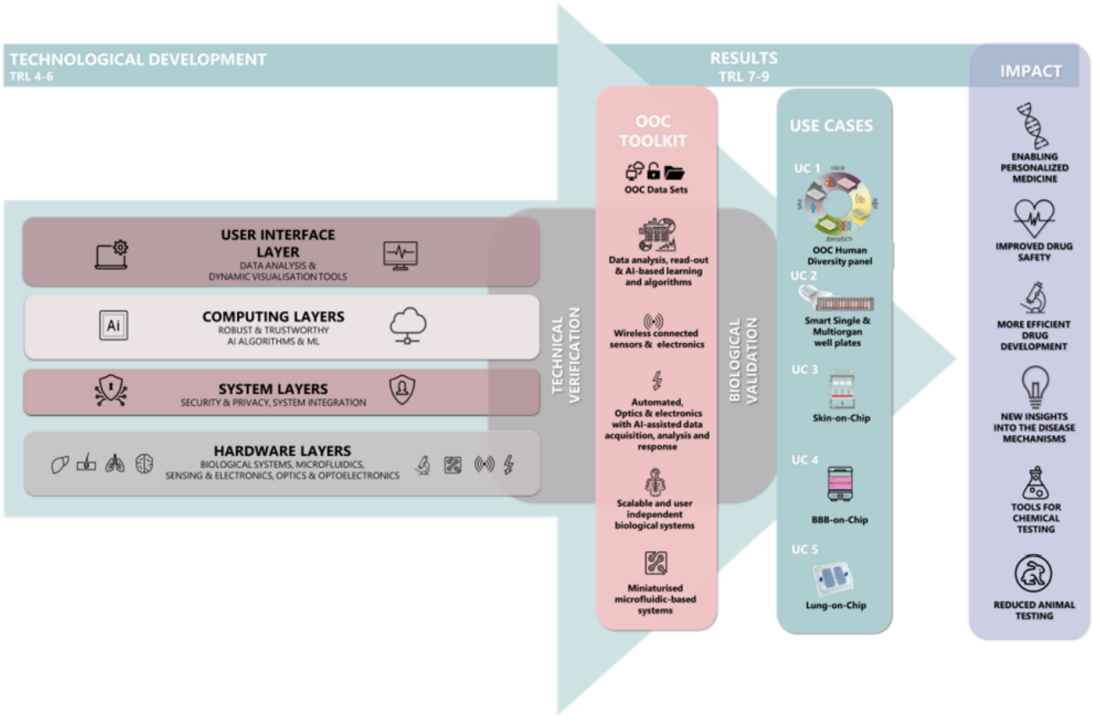


Figure 1.1: UNLOOC Project Scope, Results, Outcomes, and Impacts [3].

Despite the analog nature of such phenomenons, the transmission, storage, and processing of information are usually performed in the digital domain, using either conventional digital computers or special-purpose digital signal processors [7]. Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are essential components in this context, bridging the two data forms.

Several architectures are used to implement ADCs, being the most relevant the Flash, the Successive Approximation Register (SAR), the Pipeline, and the Sigma-Delta ($\Sigma\Delta$), each type having trade-offs between resolution, power consumption, area, sampling frequency, and the complexity of both analog and digital hardware. There is a specific interest in developing ADCs with low power consumption and minimal area for integration into large sensor matrix applications over their potential for integration with individual sensors [8]. Particularly, Sigma-Delta modulators ($\Sigma\Delta$Ms), as elaborated in Section 2.3, offer high resolution at relatively low signal bandwidths, making them particularly appealing for the UC3 due to their single serialized output and miniaturization capabilities. This opportunity offers a promising step in both ADC and OoC technologies.

1.2 Objectives

INESC-ID and INESC-MN develop a solution for well and chamber sensorization in collaboration with the other Portuguese partner that enables signal processing, including filtering and analog-to-digital conversion. This initiative involves designing integrated sensors and ASICs that fit in single wells, enabling access to complex levels of information for each well and chamber process.

The proposed system for UC3 requires low power consumption to prevent overheating and maintain stable well temperatures, low noise levels to improve the limits of detectability, and support for interfaces with resistive, capacitive, and inductive sensors. As part of the UNLOOC project, the research presented in this document aims to develop a low-area $\Sigma\Delta$M. This $\Sigma\Delta$M is implemented in TSMC $65\,\mathrm{nm}$ technology [9], selected for its state-of-the-art capabilities and accessibility within INESC-ID's research group. Specific objectives have been identified to conduct the work:

- Area: Considering technology constraints and the expected sensor size estimated by the partner organizations, a target size of $50\times50\,\mu\mathrm{m}$ is set, capable of supporting single-cell monitoring;
- Bandwidth: Given the aforementioned low bandwidth requirements of such systems, an objective of $50\,\mathrm{kHz}$ is established;
- Resolution: A resolution of $10\,\mathrm{bit}$ is considered suitable for the intended application, balancing precision with overall circuit complexity and, therefore, power consumption and silicon area utilization.

A target input dynamic range could be set at $1.2\,\mathrm{V}$ to accommodate the full range that $65\,\mathrm{nm}$ devices can withstand. However, the sensing system's input stages, such as variable-gain amplifiers or anti-aliasing filters (AAFs), ensure the effective utilization of the achieved input dynamic range of the developed modulator. Regardless, the design of such stages is outside the scope of this work.

1.3 Thesis Outline

This document is divided into 8 chapters. Following this introduction, the thesis is structured as follows:

- Chapter 2 provides a literature overview of ADCs, focusing on the essential concepts, performance metrics, and topologies relevant to this work, with particular emphasis on $\Sigma\Delta$ ADCs;
- Chapter 3 introduces a quasi-passive $\Sigma\Delta$M, outlining its architectural theory and the building blocks that form the basis for the design;
- Chapter 4 discusses porting the quasi-passive $\Sigma\Delta$M to the TSMC $65\,\mathrm{nm}$ technology. It includes detailed design adaptations, pre-layout simulations, and layout considerations;
- Chapter 5 presents the in-silicon testing and validation of the ported modulator. This chapter details wire bonding techniques and test bench setup, followed by the procedure for measuring the device's performance;
- Chapter 6 outlines simulation optimization strategies for improving the design and verification procedures. It includes simplifying the original workflow, advanced simulation techniques, and automation;

- Chapter 7 discusses the development of the final version of the $\Sigma\Delta$M. Key design optimizations are performed to enhance the circuit's performance, power efficiency, and robustness. The chapter also covers the generation of clock signals and the completion of the layout;
- Chapter 8 concludes the thesis by summarizing the contributions of the work, highlighting the main challenges encountered, and outlining areas for future improvement.

Chapter 2

Literature Review of ADCs

ADCs are crucial in converting continuous analog signals into discrete digital representations. The various ADC topologies and implementations offer flexibility to meet desired performance specifications. This chapter lays the groundwork for understanding ADCs, particularly emphasizing the $\Sigma\Delta$ topology designed to digitize low-pass (LP) signals, including an overview of some of the current state-of-the-art devices in this domain.

2.1 Basic Concepts

The process of analog-to-digital conversion for a signal is explained through two distinct operations: uniform sampling in time and quantization in amplitude [7]. This section briefly explains the essential concepts of these two aspects. Fig. 2.1 illustrates the conceptual diagram of an ADC based on three main blocks.

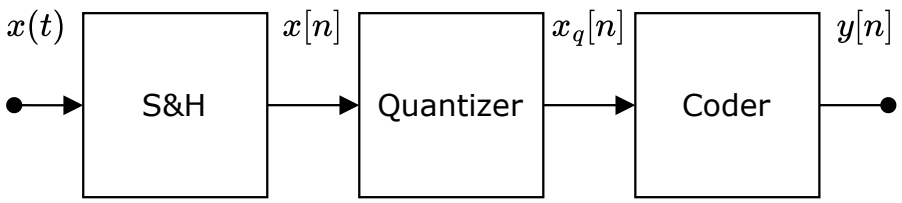


Figure 2.1: Conceptual Diagram of an ADC.

The fundamental blocks include a sample-and-hold (S&H) circuit, a quantizer, and a coder. A band-limited signal $x(t)$ is sampled at a rate f_s by the S&H circuit, resulting in a discrete-time (DT) signal $x[n]$. After the S&H process, the quantizer maps the continuous range of amplitudes of $x[n]$ into a discrete set of levels resulting in $x_q[n]$. In the final stage, the coder assigns a unique binary number to each level, generating the output digital data $y[n]$. This operation is illustrated in Fig. 2.2.

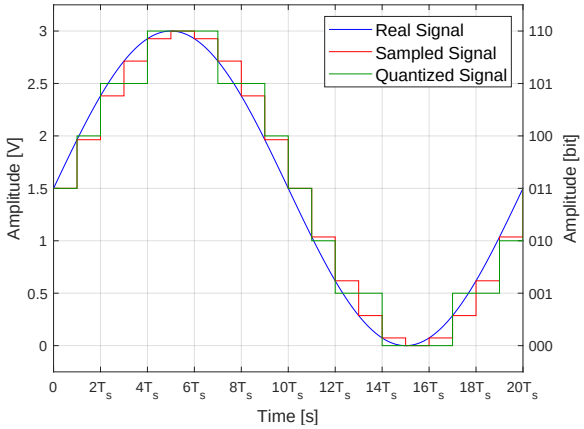


Figure 2.2: Time Domain Sampling Representation for an Example Signal.

The sampling process has the effect of periodically repeating versions of the signal spectrum at integer multiples of the sampling frequency $f_s = 1/T_s$, as seen in (2.1), where $X_s(f)$ represents the spectrum of the sampled signal and $X(f)$ is the spectrum of the original continuous-time (CT) signal $x(t)$.

$$X_s(f) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X(f - k f_s) \tag{2.1}$$

Generally, the signal can be reconstructed back to continuous time if the repeated versions of the signal spectrum, so-called replicas, do not overlap. According to the Nyquist theorem, the sampling frequency f_s should be at least twice the signal bandwidth f_B, denoted as $f_N = 2f_B$, to ensure signal reconstruction and avoid replica overlap, also known as aliasing. At $f_s = f_N$, an ADC operates as a Nyquist-rate ADC; however, if f_s exceeds f_N, it becomes an oversampling ADC. The oversampling ratio (OSR), assumed to be an integer, is given by $\mathrm{OSR} = f_s/f_N > 1$.

$\Sigma\Delta$ ADCs are designed to operate using oversampling and, as shown in Fig. 2.3, their fundamental structure consists of two main blocks [10]. The $\Sigma\Delta$M, which includes an integrator, an internal ADC or quantizer, and a DAC within the feedback loop, performs both oversampling and quantization of the band-limited input signal. The quantization error undergoes high-pass filtering using specific noise-shaping techniques, as later described in Sections 2.4 and 3.1.3. The $\Sigma\Delta$M outputs a B-bit digital stream at a sampling rate f_s, occasionally referred to as a standalone ADC for this exact reason. The decimator reduces the $\Sigma\Delta$M output stream rate to the Nyquist rate. Simultaneously, the word length increases from B to N to maintain resolution while decreasing the word rate. The decimator's high-selectivity digital filter eliminates frequency components of the stream above f_B.

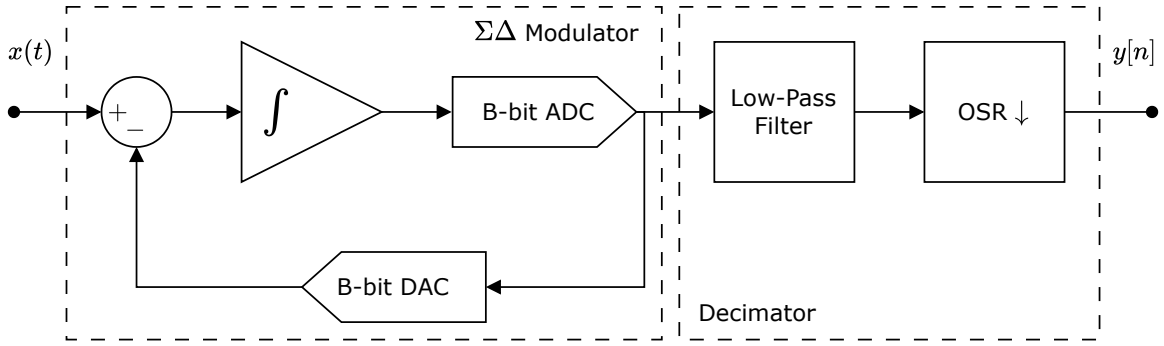


Figure 2.3: Conceptual Diagram of a $\Sigma\Delta$ ADC.

2.2 Performance Metrics

There are various parameters for characterizing the performance of ADCs across different domains. Understanding and optimizing these parameters leads to accurate and reliable signal conversion. Designers must balance these parameters to meet the specific requirements of the intended application while considering the trade-offs involved in achieving optimal performance. In the present work's context, the most important metrics that define ADCs are:

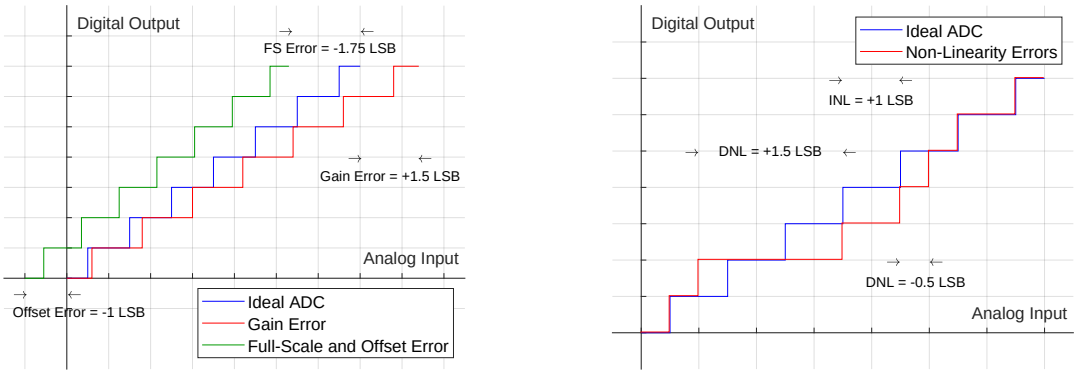
- Area: The converter's total physical space on a semiconductor chip;
- Sampling Frequency: The rate at which the ADC captures and converts the analog signals;
- Bandwidth: The spectrum of frequencies within the analog input signal that an ADC can capture and convert. As detailed in Section 2.1, this bandwidth is constrained by the sampling frequency;
- Resolution: Number of digital bits produced per analog signal sample. Higher resolution leads to finer granularity in signal representation. N-bit resolution corresponds to 2^N digital levels;
- Dynamic Range: The range of signal amplitudes that the ADC can resolve. If the signal is too large, it over-ranges the ADC input. If the signal is too small, it gets lost in the converter's quantization noise. Alternatively, the ADC's dynamic range can also be defined as the range between the noise floor of a device and its specified maximum output level [11];
- Latency: It is the time delay between a change in the analog input signal and the corresponding output in the digital domain;
- Power Consumption: The amount of electrical energy the ADC consumes during operation.

2.2.1 Static Parameters

The static parameters comprise offset, gain, and full-scale (FS) errors, each referred to as linear errors. Additionally, there are non-linear error counterparts, namely integral and differential errors. Fig. 2.4 shows the corresponding graphic representations [12].

The offset error is the constant direct current (DC) offset between the ADC's transfer function and the ideal transfer function, as illustrated in Fig. 2.4(a), where the green line exhibits $-1\,\mathrm{LSB}$ of offset error. Gain error represents the deviation in slope of the transfer function from the ideal transfer function, as depicted in Fig. 2.4(a), where the red line shows around $1.5\,\mathrm{LSB}$ of gain error. Lastly, FS error denotes the maximum deviation of the ADC's transfer function from the ideal transfer function, as seen in Fig. 2.4(a), where the green line displays $-1.75\,\mathrm{LSB}$ of FS error. Since there is no offset error on the red line, the FS error is the same as the gain error.

Integral non-linearity (INL) error quantifies the maximum deviation of the ADC's transfer curve from the ideal function at various states. On the other hand, differential non-linearity (DNL) error measures the maximum deviation between the actual and ideal step sizes between two adjacent codes. Fig. 2.4(b) illustrates the impact of these two metrics on the transfer characteristic of an ADC.



(a) Linear Errors

(b) Non-Linear Errors

Figure 2.4: Effect of Errors on ADC Transfer Characteristic.

Finally, monotonicity stands as an important parameter. An ADC is considered monotonic if the digital output code also increases for increasing analog voltage input, and vice versa. Monotonic behavior, however, does not guarantee the absence of missing codes. A converter is guaranteed to be monotonic if the DNL error is no greater than $\pm 1\,\mathrm{LSB}$. It is important to note that even in the case of a monotonic ADC, a DNL greater than $1\,\mathrm{LSB}$ could still lead to the occurrence of missing code(s) at certain points in the transfer function [12].

2.2.2 Dynamic Parameters

The dynamic parameters include Total Harmonic Distortion (THD), Signal-to-Noise Ratio (SNR), Signal-to-Noise-and-Distortion Ratio (SNDR), and Effective Number of Bits (ENOB). The parameters described apply to a signal with specified amplitude and frequency, following the IEEE standards [13].

THD quantifies the root sum of squares (RSS) of harmonic distortion components, including their aliases, in the spectral output of the ADC. Typically, THD is estimated by considering the RSS of the second through tenth harmonics V_i. THD is often expressed in decibels (dB) relative to the root mean square (RMS) amplitude of the output component at the input frequency V_1, also known as the first harmonic, as seen in (2.2).

$$\mathrm{THD} = 20\log_{10}\left(\frac{\sqrt{\sum_{i=2}^{10} V_i^2}}{V_1}\right) \ [\mathrm{dB}] \tag{2.2}$$

SNR measures the ratio of V_1 to the RMS amplitude of the output noise V_n. This ratio, seen in (2.3), excludes the harmonic distortion components considered in THD.

$$\mathrm{SNR} = 20\log_{10}\left(\frac{V_1}{V_n}\right) \ [\mathrm{dB}] \tag{2.3}$$

The relationship between the RMS amplitude of the output signal from the ADC and the RMS amplitude of the output noise represents SNDR, also referred to as SINAD [7, 11]. In this context, noise includes random errors, non-linear distortion, and all the impacts of sampling errors, as seen in (2.4).

$$\mathrm{SNDR} = 20\log_{10}\left(\frac{V_1}{\sqrt{V_n^2 + \sum_{i=2}^{10} V_i^2}}\right) \ [\mathrm{dB}] \tag{2.4}$$

ENOB signifies the bit count that matches the quantization noise level of the actual converter. ENOB characterizes the dynamic resolution of an ADC and its calculation is given by (2.5).

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02} \ [\mathrm{bit}] \tag{2.5}$$

2.2.3 Figures-of-Merit

Figure-of-Merit (FoM) is a numerical quantity based on one or more characteristics of a system or device that represents a measure of efficiency or effectiveness. Various authors employ different methods to calculate FoMs [11, 14, 15], with the most widely used approaches for ADCs outlined in (2.6) and (2.7). In this context, P_w is the power consumption of the converter, f_B stands for bandwidth, and SNDR and ENOB are defined in (2.4) and (2.5), respectively. These FoMs can be expressed in both linear and logarithmic forms [16].

$$\mathrm{FoM}_1 = \mathrm{SNDR} + 10\log_{10}\left(\frac{f_B}{P_w}\right) \ [\mathrm{dB}] \tag{2.6}$$

$$\mathrm{FoM}_2 = \frac{P_w}{2 \cdot f_B \cdot 2^{\mathrm{ENOB}}} \ [\mathrm{fJ/conv-step}] \tag{2.7}$$

Notably, FoM_1 emphasizes effective resolution, whereas FoM_2 emphasizes power consumption [17]. Therefore, the larger the FoM_1 value and the smaller the FoM_2 value, the more favorable the ADC is. In the context of this work, where area is a crucial metric, defined as A, an alternative FoM is used, as shown in (2.8) [18].

$$\mathrm{FoM}_3 = \frac{P_w \cdot A}{2 \cdot f_B \cdot 2^{\mathrm{ENOB}}} \ [\mathrm{fJ \cdot mm^2/conv-step}] \tag{2.8}$$

In Section 2.5, an analysis is conducted on the last two FoMs' applicability in characterizing different categories of ADCs. The study also identifies the FoM thresholds at which an ADC demonstrates significant performance.

2.3 Topology Selection Criteria

The various ADC topologies present advantages and limitations across the different performance metrics outlined in Section 2.2. Fig. 2.5 visually represents the relationship between resolution and bandwidth, highlighting the clustering of different ADC types within specific regions.

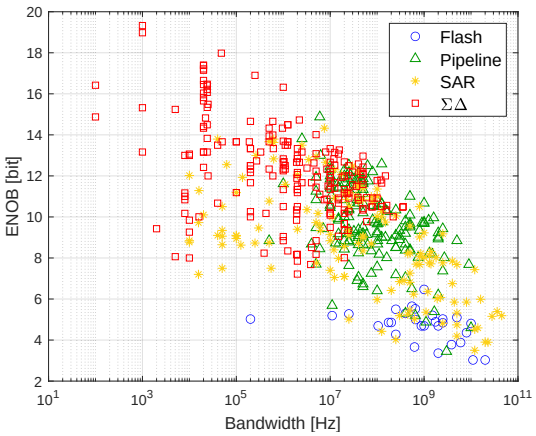


Figure 2.5: Resolution vs. Bandwidth Analysis for Different ADC Topologies.

As shown in Fig. 2.5, $\Sigma\Delta$ ADCs provide the highest resolution for relatively low signal bandwidths. Nevertheless, different implementations have enabled their use in medium to high-frequency applications with reduced resolution. $\Sigma\Delta$ ADCs span a wide range of specifications, accommodating frequencies from $100\,\mathrm{Hz}$ to $360\,\mathrm{MHz}$ and an ENOB ranging from 7 to $20\,\mathrm{bit}$. Conventional ADC types such as Flash, SAR, and Pipeline are preferred for high-speed applications, as they can handle signal bandwidths well above $1\,\mathrm{MHz}$.

Multiple $\Sigma\Delta$ converters with ENOB exceeding $10\,\mathrm{bit}$ for the bandwidth of $50\,\mathrm{kHz}$ (established as a goal in Section 1.2) can be observed in Fig. 2.5. These results suggest that a converter with an ENOB of $10\,\mathrm{bit}$, within

the same bandwidth and using $\Sigma\Delta$ techniques, is expected to offer advantages in terms of area and power consumption. Thus, the $\Sigma\Delta$ ADC topology is considered most suitable for minimizing area and power requirements.

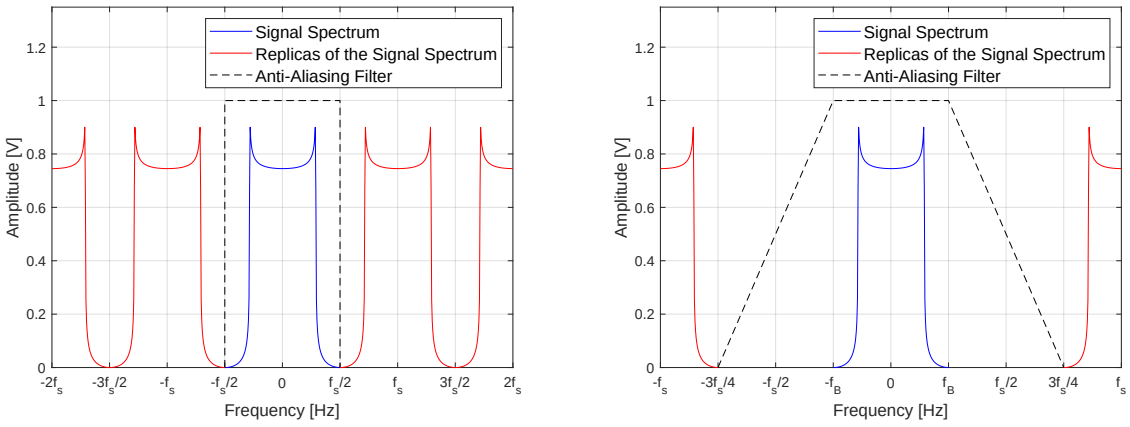
Further, a $\Sigma\Delta$ ADC or modulator can be selected. A modulator is sufficient because it provides a single serialized digital output, leading to a more compact design and lower power consumption. However, additional post-processing is necessary to achieve complete digitization, involving, for example, a field-programmable gate array (FPGA) to implement a decimator filter.

2.4 Fundamentals of $\Sigma\Delta$ ADCs

Integrating oversampling and noise shaping in ADCs enhances resolution, simplifies AAF requirements, and reduces in-band noise power, thereby improving performance [11]. This section explores the core principles behind $\Sigma\Delta$ ADCs, explaining the processes of oversampling, noise shaping, and decimation.

2.4.1 Oversampling

Oversampling ADCs offer advantages, notably in simplifying the requirements of the AAF generally employed at the input of the ADC, compared to Nyquist-rate ADCs. Nyquist-rate ADCs demand a sharp AAF transition band, seen in Fig. 2.6(a), introducing phase distortion [11]. Oversampling ADCs with a higher OSR simplifies AAF requirements, as exemplified in Fig. 2.6(b), reducing distortion.



(a) Nyquist-rate ADC

(b) Oversampling ADC

Figure 2.6: Frequency Domain Representation for different Sampled Signals.

Another benefit is the reduction of in-band noise power. In Nyquist-rate ADCs, the in-band noise power remains constant, but with oversampling, it decreases with OSR at a $3\,\mathrm{dB/octave}$ rate, as proven by several studies [7, 11, 19, 20]. In other words, oversampling distributes quantization noise power over a larger frequency band, attenuating in-band quantization noise compared to Nyquist-rate ADCs.

2.4.2 Noise Shaping

The accuracy of an ADC can be enhanced by filtering the quantization noise so that most of its power lies outside the signal band. The quantization error, the difference between the input signal and the ADC output in an analog representation, is shaped by a filter. Said filter's transfer function is typically a high-pass filter, attenuating noise around DC. For LP oversampled signals, low-frequency in-band components of the quantization error can be attenuated by applying a differentiator filter with a Z-domain transfer function, which is a function of the filter order L [11]. The quantization noise power in for the band of interest exhibits a decrease with the OSR at a rate of roughly $6L\ \mathrm{dB/octave}$ beyond that achieved by oversampling alone [11]. These filtering techniques are essential and will be analyzed in more detail in Section 3.1.3 when evaluating a $\Sigma\Delta$M transfer function.

2.4.3 Decimation

In $\Sigma\Delta$ ADCs, a B-bit data stream transforms into N-bit word through decimation. This process begins with an averaging operation, wherein the bit stream is accumulated over a fixed duration and the total is divided by the number of periods, leading to an increase in data resolution from B-bit to N-bit representation. The averaging operation is equivalent to the effect of a low-pass filter (LPF). Once the signal is band-limited by the LPF, decreasing the sampling rate without introducing aliasing becomes possible. The sampling rate $f_s = 2 \cdot \mathrm{OSR} \cdot f_B$ is reduced to f_s/OSR, with OSR being an integer, also known as the decimation factor. The combined process of LP filtering and downsampling is referred to as decimation [21].

2.5 State of the Art in Compact $\Sigma\Delta$ ADCs

This section provides an overview of recent state-of-the-art $\Sigma\Delta$ ADCs, with a particular emphasis on integrated circuits (ICs) realized in nanometer-scale (smaller than $180\,\mathrm{nm}$) technologies. The analysis is based on converters documented in the ADC survey by Boris Murmann, covering the period from 1997 to 2024 [14].

2.5.1 General Overview

The present study aims to identify converters that minimize power consumption and chip area. The relationship between area and power shown in Fig. 2.7 highlights a trend where an appealing trade-off between minimal area and low power consumption can be observed, particularly in the region below the gray dashed line. Among the circuits in this area, the six most recent are selected for further discussion in the following sections.

The focus of FoM_1 is effective resolution, while FoM_2 prioritizes power consumption, and FoM_3 also focuses on the total chip area, as outlined in Section 2.2.3. These six circuits provide high performance based on FoM_2 or FoM_3, or both, placing them in the top $5\,\%$ of the analyzed devices [14]. The circuits are categorized into high and low resolution, based on an ENOB threshold of $10\,\mathrm{bit}$, to facilitate the analysis.

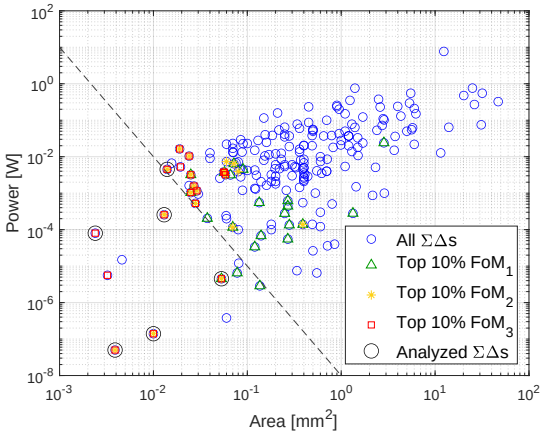


Figure 2.7: Area vs. Power Consumption Analysis for $\Sigma\Delta$ ADCs.

2.5.2 High Resolution

The 3rd-order, 1-bit CT $\Sigma\Delta$M presented by João de Melo et al. employs a loop filter consisting of passive resistor-capacitor (RC) integrators and a single feedback path [22]. Differential pairs are added between the passive RC integrators to avoid the loading effect of the following stage. The comparator design includes a preamplifier stage formed by a differential pair with a resistive load, followed by a latch and a D flip-flop. The modulator's architecture utilizes only differential pairs and positive feedback in the comparator, allowing for low power consumption and operation at reduced supply voltages. Additionally, these circuits occupy less area than high-gain, wide-bandwidth amplifiers with complex compensation schemes. The modulator achieves an ENOB of $11.2\,\mathrm{bit}$ for a $2\,\mathrm{MHz}$ bandwidth, with a power consumption of $256\,\mu\mathrm{W}$ and an area of $0.013\,\mathrm{mm}^2$.

The design of a 0-1 Multi-Stage Noise Shaping (MASH) $\Sigma\Delta$ ADC is introduced by Yan Song et al. [23]. The proposed design incorporates alternate loading capacitors (ALC) for error feedback, resulting in an ideal 1st-order noise-shaping process. In this architecture, the ADC's first stage can undergo sampling and conversion during the second stage integration, enabling pipeline operation with a bandwidth reaching up to $12.5\,\mathrm{MHz}$. The robustness of the noise transfer function and noise cancellation filter accuracy is maintained, as they depend solely on the capacitor ratio and remain resilient to process variations. The modulator featuring ALC can be realized by reconfiguring the conventional pipelined SAR structure without incurring additional area overhead. The ENOB achieved is $12.5\,\mathrm{bit}$, with a total area of $0.014\,\mathrm{mm}^2$ and a power consumption of $4.5\,\mathrm{mW}$.

Hariprasad Chandrakumar et al. present a $\Sigma\Delta$M architecture that incorporates a 3rd-order cascade of integrators with feedforward summation loop filter, while the quantizer is a 6-bit SAR ADC [24]. In the first integrator stage, an inverting amplifier with capacitive feedback is used to ensure power efficiency and chopping techniques are implemented to mitigate flicker noise. The loop-filter operational amplifiers (OPAMPs) are designed as two-stage Miller-compensated OPAMPs. A capacitively coupled chopper instrumentation amplifier with a gain of 8 is also designed for the front-end. The peak ENOB is $15.3\,\mathrm{bit}$ in a signal bandwidth of $5\,\mathrm{kHz}$, consuming $4.5\,\mu\mathrm{W}$ and occupying an area of $0.053\,\mathrm{mm}^2$. Disabling the proposed techniques, including time-varying

degeneration, reference-buffer assist, and dead-band switches, results in a reduction of ENOB to $9.7\,\mathrm{bit}$ due to increased distortion, demonstrating the effectiveness of these techniques in maintaining system performance.

These descriptions suggest that high resolution in $\Sigma\Delta$ converters requires amplification. This amplification often increases power consumption, particularly for systems with high bandwidth requirements. However, since power consumption is frequency dependent [25], achieving high resolution with low power consumption is possible if the bandwidth is sufficiently low, as demonstrated by the last circuit presented [24].

2.5.3 Low Resolution

A compact and low-power current-input $\Sigma\Delta$ topology is proposed by Maged El Ansary et al. [26]. The input current and a simple charge-sharing DAC integrate onto a grounded integration capacitor as an alternative to an active integrator, such as a transimpedance amplifier (TIA). Noise-shaping techniques ensure that harmonics generated by clock signals only manifest at higher frequencies. The ADC effectively rejects in-band noise, including DC offset and $1/f$ noise introduced by the comparator, with its transfer function closely resembling that of an active-integrator $\Sigma\Delta$ ADC. Furthermore, adjusting capacitor sizes facilitates charge transfer between a smaller capacitor from the DAC and the larger integration capacitor, based on the comparator output, without using an OPAMP. Power efficiency is enhanced by the low duty cycle of the comparator, resulting in the lower power consumption among the $\Sigma\Delta$ converters at $50\,\mathrm{nW}$ with a $5\,\mathrm{kHz}$ bandwidth, an ENOB of $8.1\,\mathrm{bit}$ and $0.0039\,\mathrm{mm}^2$ of area.

The 2$^{\text{nd}}$-order $\Sigma\Delta$ ADC, also documented by Maged El Ansary, is implemented as a singular loop comprising two passive integrators, a comparator, and a 1-bit charge-pump DAC [27]. Similar to the previous circuit [26], this ADC achieves power savings by replacing amplifiers with passive integrators and using a charge-pump without an OPAMP. Despite the power-saving modifications, the primary noise contributors are the flicker noise and offset of the comparator. These noise sources are, however, modulated to higher frequencies and noise-shaped to the 2$^{\text{nd}}$ order, together with quantization noise. The ADC achieves an ENOB of $8\,\mathrm{bit}$ for a $10\,\mathrm{kHz}$ bandwidth while consuming $140\,\mathrm{nW}$ and an area occupation of $0.01\,\mathrm{mm}^2$.

A quasi-passive 1$^{\text{st}}$-order $\Sigma\Delta$M is introduced by Gonçalo Rodrigues et al. [28]. This circuit employs a transconductor to convert the input voltage into a current, which is then integrated as charge into the gate capacitance of a MOS capacitor (MOSCAP). The device leverages the variable capacitance of MOSCAP to minimize charge leakage during integration. Moreover, its transconductor-based front-end offers a sinc filter response, enhancing tolerance to clock jitter, time skew, non-zero rise and fall times of the sampling clock, and switch resistance compared to traditional track-and-hold (T&H) methods. Additionally, by appropriately biasing the MOSCAPs, the inherent negative feedback loop of the $\Sigma\Delta$M ensures integration in the minimal charge loss zone. The proposed topology is verified through simulation using a $130\,\mathrm{nm}$ technology. The resolution, however, is constrained by the non-linear nature of passive integration attributed to MOSCAP parasitic capacitances. The circuit achieves an ENOB of $8.2\,\mathrm{bit}$ for a bandwidth of $390.625\,\mathrm{kHz}$, with the smallest area reported in the literature at $0.0024\,\mathrm{mm}^2$ and a power consumption of $80\,\mu\mathrm{W}$.

The $\Sigma\Delta$ converters discussed in this section operate without explicit amplification, leading to lower resolution than the previously described devices. However, in some cases, their power consumption is lower, by 4 to 5 orders of magnitude. The absence of amplification and the reduced loop filter order also enable compact implementations, as these converters occupy similar or much smaller area than the ones in the last subsection.

2.5.4 Comparative Analysis

Tab. 2.1 summarizes the performance of the state-of-the-art $\Sigma\Delta$ ICs examined in this study. The arrangement of the table columns is based on the publication date of the respective papers.

Table 2.1: State-of-the-Art Small $\Sigma\Delta$ Converters Performance Comparison.

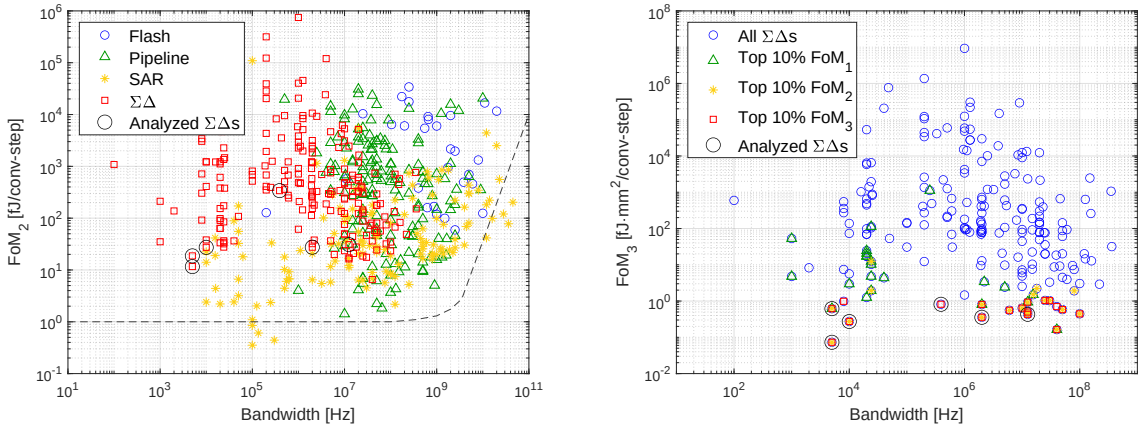
Reference	[22]	[23]	[24]	[26]	[28]	[27]
Year	2015	2018	2018	2018	2019	2021
Type	$\Sigma\Delta$M	$\Sigma\Delta$ ADC	$\Sigma\Delta$ ADC	$\Sigma\Delta$ ADC	$\Sigma\Delta$M	$\Sigma\Delta$ ADC
Architecture	CT	0-1 MASH	CT	OpAmp-Less	DT Quasi-Passive	OpAmp-Less
Loop Filter Order	3rd	1st	3rd	1st	1st	2nd
Technology [nm]	65	65	40	130	130	130
Area [mm^2]	0.0130	0.0140	0.0530	0.0039	0.0024	0.0100
Samp. Frequency [MHz]	320.000	200.000	0.400	0.846	100.000	2.000
Bandwidth [kHz]	2000	12500	5	5	391	10
ENOB [bit]	11.2	12.5	15.2	8.1	8.2	8.0
Power Consumption [μW]	256.00	4500.00	4.50	0.05	80.00	0.14
FoM$_2$ [$\mathrm{fJ/conv-step}$]	27.5	30.8	11.6	18.7	339.7	27.3
FoM$_3$ [$\mathrm{fJ\cdot mm^2/conv-step}$]	0.357	0.431	0.617	0.073	0.815	0.273

The minimum values for FoM$_2$ and FoM$_3$ are $11.6\,\mathrm{fJ/conv-step}$ and $0.073\,\mathrm{fJ\cdot mm^2/conv-step}$ for the circuits referenced from Hariprasad Chandrakumar [24] and Maged El Ansary [26], respectively. Establishing criteria for a good or bad FoM involves more than assigning a numerical value. For instance, as illustrated in Fig. 2.8(a), a clearly defined envelope limits FoM$_2$ at higher frequencies. For a bandwidth range from $20\,\mathrm{kHz}$ to $500\,\mathrm{kHz}$, a FoM$_2$ of $20\,\mathrm{fJ/conv-step}$ or lower is considered favorable. This range represents the performance of $10\,\%$ of the converters reported in the literature. The same principle is applied to the FoM$_3$, with a threshold of $1\,\mathrm{fJ\cdot mm^2/conv-step}$ established as a suitable criterion. These reference values are presented in Tab. 2.2.

Table 2.2: Reference Values for FoM$_2$ and FoM$_3$.

FoM$_2$	**FoM$_3$**
$20\,\mathrm{fJ/conv-step}$	$1\,\mathrm{fJ\cdot mm^2/conv-step}$

Three out of the six circuits highlighted are specifically designed for applications in the nervous system [24, 26, 27]. Power efficiency is a crucial cost factor in these applications, with the relevant bandwidth ranging from $1\,\mathrm{Hz}$ to $5\,\mathrm{kHz}$ [6, 29]. Remarkably, these implementations demonstrate exemplary performance in both FoMs studied.



(a) FoM_2 for Various Types of Converters

(b) FoM_3 for $\Sigma\Delta$ Converters

Figure 2.8: FoMs vs. Bandwidth Analysis.

Finally, there is a gap in $\Sigma\Delta$ converters within the bandwidth range of $25\,\text{kHz}$ to $350\,\text{kHz}$ concerning acceptable FoMs, as shown in both images from Fig. 2.8, indicating an opportunity for a meaningful scientific contribution. The circuit described by Gonçalo Rodrigues [28] is of particular interest for this work as it is the smallest area $\Sigma\Delta$ converter identified [14]. The circuit's performance metrics reveal that the FoM_2 is inadequate, exceeding the acceptable threshold by one order of magnitude, set at $334\,\text{fJ/conv}-\text{step}$, thereby indicating improvement potential. In contrast, the FoM_3 falls within adequate boundaries, suggesting that future studies should prioritize enhancements in power management. This $\Sigma\Delta$M also benefits from the continued availability of its original design team and files, having been proposed from within the INESC-ID research group in 2019. Accordingly, this circuit is selected for further development and adaptation in the present document to enhance its FoMs and meet the objectives specified in Section 1.2.

Chapter 3

The Quasi-Passive ΣΔ Modulator

After analyzing different ΣΔ topologies, a quasi-passive 1st-order ΣΔM topology is selected for further development and study. This ΣΔM architecture exhibits low power consumption and occupies a minimal area due to the absence of OPAMPs. This chapter introduces the reference ΣΔM architecture, detailing its components, presenting schematics, and concluding with an explanation of its operating principles.

3.1 Architectural Theory

A ΣΔM consists of an integrator, an ADC or quantizer, and a DAC within the feedback loop, as illustrated in Fig. 3.1 and elaborated in Section 2.1. This section provides an overview of concepts related to ΣΔ modulation, beginning with an examination of the integrator architecture of the reference circuit and subsequently analyzing the transfer function of the complete ΣΔM [28].

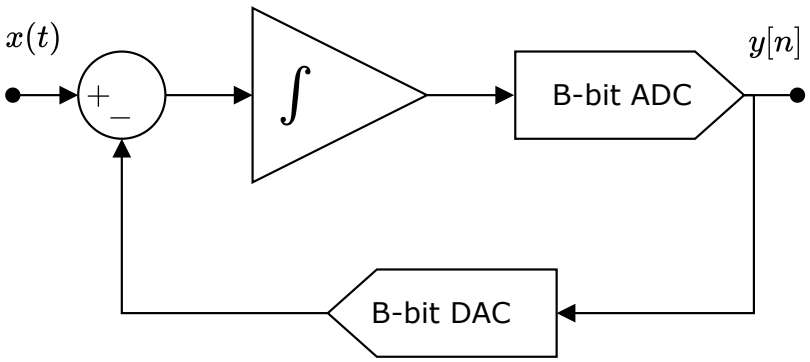


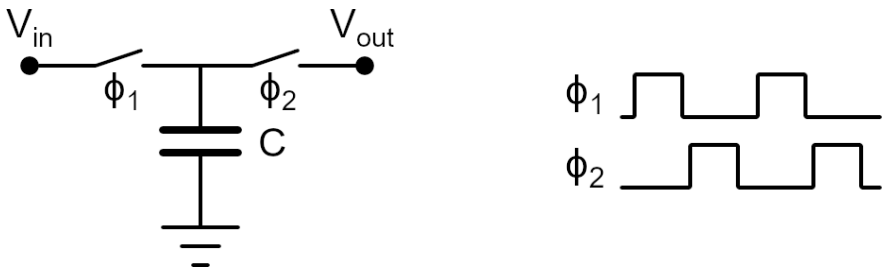
Figure 3.1: Conceptual Diagram of a 1st-order ΣΔM.

Models are useful for understanding and analyzing circuits, but their limitations should be considered when interpreting results or applying them to practical scenarios, as no model can perfectly represent reality. The DT models in this section neglect factors such as parasitic effects, temperature and clock variations.

3.1.1 Switched Capacitor Integration

In complementary metal-oxide semiconductor (CMOS) technology, resistors are commonly replaced by switched capacitors (SCs), leading to more compact and area-efficient designs. One SC resistor consists of a capacitor and two switches, controlled by two non-overlapping clock signals, ϕ_1 and ϕ_2, as shown in Fig. 3.2. The capacitor alternates between charging and discharging according to the switching frequency, and at sufficiently high frequencies, it behaves similarly to a resistor. The equivalent resistance of the SC is defined by (3.1), where f_ϕ denotes the phases frequency and C the SC capacitance [30].

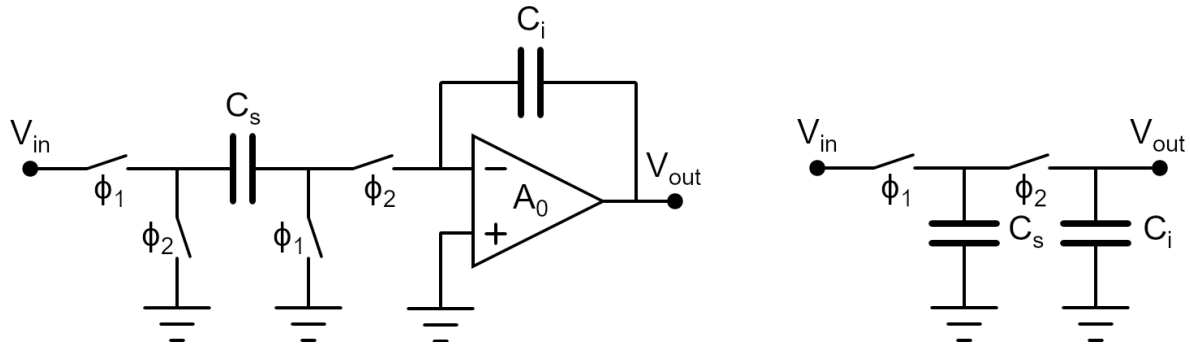
$$R_{eq} = \frac{1}{C \cdot f_\phi} \tag{3.1}$$



(a) Circuit Configuration **(b)** Non-Overlapping Clocks

Figure 3.2: SC Resistor Implementation.

This principle of using SCs can also be applied to the design of integrators. A typical SC integrator using an OPAMP is depicted in Fig. 3.3(a). The dynamic performance of the OPAMP, such as its unity-gain bandwidth and slew rate, influences the speed of integration, while the DC voltage gain impacts integration accuracy [28, 31].



(a) Active Integrator **(b)** Passive Integrator

Figure 3.3: SC Integrator Configurations.

The non-delaying transfer function of the integrator shown in Fig. 3.3(a) is given by (3.2) [32]. The parameter β, considering an active integrator, is defined in (3.3). Where A_0 represents the OPAMP's DC voltage gain, C_s is the sampling capacitor, and C_i is the integration capacitor, as seen in Fig. 3.3(a).

$$H_i(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{\alpha}{1-\beta z^{-1}} \tag{3.2}$$

$$\beta_1 = \frac{C_i + C_i \cdot A_0}{C_s + C_i + C_i \cdot A_0} \tag{3.3}$$

In the ideal case where $A_0 = \infty$, $\alpha_1 = C_s/C_i$ and $\beta_1 = 1$. When the OPAMP has a finite A_0, integration leakage occurs, resulting in a lossy SC integrator, with $\beta_1 < 1$. This leakage reduces the noise-shaping capabilities of $\Sigma\Delta$Ms, leading to a reduction in the SNDR [31].

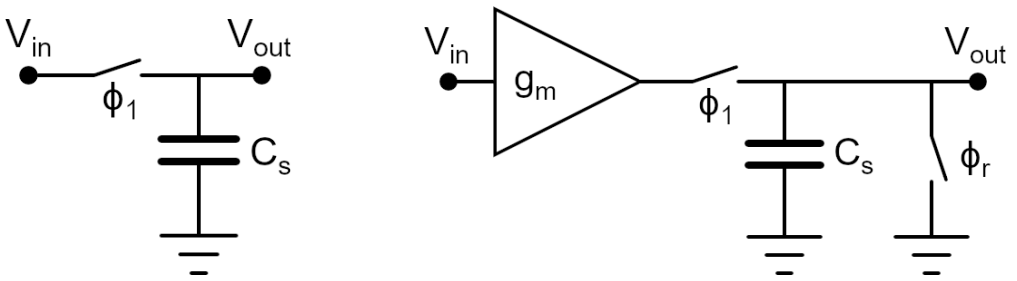
A passive SC integrator, depicted in Fig. 3.3(b), can be used to avoid power-hungry amplifiers and the complexity of OPAMP design [31]. Like the active implementation, this circuit uses two switches controlled by non-overlapping clocks, ϕ_1 and ϕ_2. During ϕ_1, the input signal is sampled onto C_s, and during ϕ_2, the charge is transferred to capacitor C_i. Before the next integration cycle begins, C_s is disconnected from C_i. However, while the voltage across C_i remains unchanged by disconnecting C_s, charge loss occurs due to the non-zero capacitance of C_s. This results in integration performance degradation similar to the leakage caused by finite OPAMP gain in an active SC integrator. For the passive integrator shown in Fig. 3.3(b), α_2 and β_2 are given by (3.4) [28].

$$\alpha_2 = \frac{C_s}{C_s + C_i} \quad \wedge \quad \beta_2 = \frac{C_i}{C_s + C_i} \tag{3.4}$$

In (3.4), α_2 is always less than 1, attenuating the input signal. The parameters β_1 and β_2 are identical when $A_0 = 0$, which is expected since passive integrators do not use amplifiers [28]. The absence of A_0 in β_2 makes designing high-accuracy passive integrators, and thus passive $\Sigma\Delta$Ms, more challenging.

3.1.2 The Integrator Front-End

The combination of the first switch and the capacitor C_s in Fig. 3.3(b) is commonly referred to as the T&H circuit, depicted in Fig. 3.4(a), which serves as the front-end in certain ADCs. As illustrated in Fig. 3.5, a clock signal ϕ_1, controls the switch to begin and end the tracking phase. During the tracking phase, the capacitor tracks the input voltage V_{in}, and during the hold phase, the output voltage V_{out}, is maintained at the sampled value.

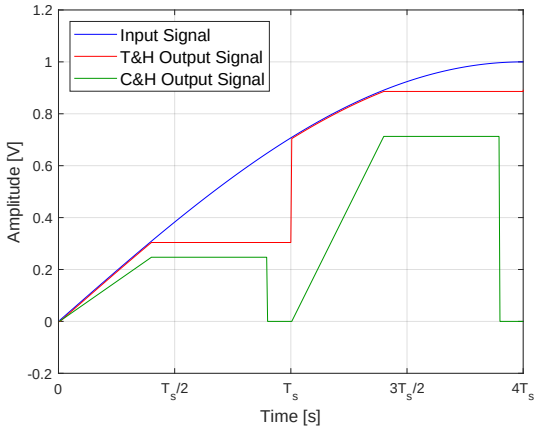


(a) Track-and-Hold Circuit

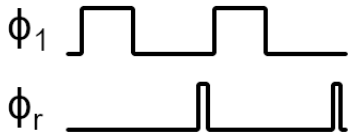
(b) Charge-and-Hold Circuit

Figure 3.4: Integrator Front-End Configurations.

An alternative to the T&H circuit is the charge-and-hold (C&H) circuit, also referred to as the integrator-and-hold [28], which operates in the charge domain. Fig. 3.4(b) depicts the C&H circuit, which comprises a transconductance (g_m) cell, a reset switch, a capacitor, and a control switch. The g_m cell, converts the input voltage V_{in} to a current, as given by (3.5), which is then integrated into the capacitor over time. Unlike the T&H, this current-based circuit transfers signals in terms of charge and is more tolerant to clock jitter, time skew, and switch resistance due to the C&H's inherent sinc filter response [33].



(a) Input and Output Waveforms



(b) Control Clocks

Figure 3.5: Comparison of Integrator Front-End Configurations.

$$I = G_m \cdot V_{in} \tag{3.5}$$

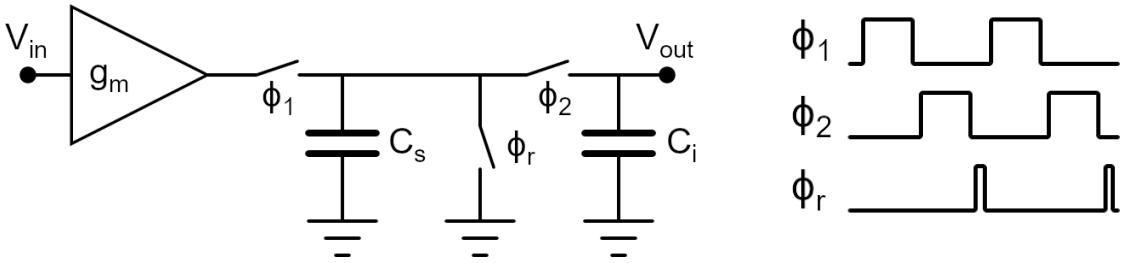
When the C&H operates in current mode, the charge transferred to the capacitor is linearly dependent on the input voltage. However, as the capacitor voltage approaches the g_m cell output voltage, the current decreases, and the capacitor voltage begins to track the input voltage, transitioning the circuit into voltage mode. In this mode, the charge is no longer linearly dependent on the current, which degrades the linearity of the $\Sigma\Delta$M and reduces the SNDR. Therefore, maintaining the C&H in current mode is essential for optimal $\Sigma\Delta$M resolution.

Assuming the g_m cell is an ideal transconductor with transconductance G_m, V_{in} is a DC voltage because f_s is significantly greater than the input bandwidth and δ is the duty cycle ratio of ϕ_1, the charge transferred can be expressed as in (3.6).

$$Q_s = \int_0^{\delta T_s} I dt = \int_0^{\delta T_s} (V_{in} \cdot G_m) dt = V_{in} \cdot \delta T_s \cdot G_m \tag{3.6}$$

3.1.3 Transfer Function

By reviewing the gathered information, a simplified version of the integrator from the reference circuit can be presented, as shown in Fig. 3.6. The non-overlapping control clocks are depicted in Fig. 3.6(b).



(a) Simplified Circuit **(b)** Control Clocks

Figure 3.6: Configuration of the Reference Integrator.

As discussed in Section 2.4, the integrator operates as the filter in most DT $\Sigma\Delta$M architectures [7]. Notably, analyzing the integrator is beneficial to derive the transfer function of the complete $\Sigma\Delta$M implementation, as its behavior directly affects the overall system's transfer function.

The integration process begins by considering the charge equation in (3.6) during the period when ϕ_1 is active. The initial charge stored in C_i from the previous cycle is provided by (3.7). In the subsequent phase, when ϕ_2 is active within the same clock period, the charge in C_s is transferred to C_i, as described in (3.8). By replacing (3.6) and (3.7) into the overall charge balance equation, (3.8), the final expression in (3.9) is obtained. The conversion of this expression to the Z-domain results in the transfer function shown in (3.10), as expected and seen in Section 3.1.1.

$$Q_i[n-1] = V_{out}[n-1] \cdot C_i \tag{3.7}$$

$$Q_{out}[n] = Q_s[n] + Q_i[n-1] = V_{out}[n] \cdot (C_s + C_i) \tag{3.8}$$

$$V_{out}[n] \cdot (C_s + C_i) = V_{in}[n] \cdot \delta T_s \cdot G_m + V_{out}[n-1] \cdot C_i \tag{3.9}$$

$$H_{qp}(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{\alpha_3}{1-\beta_3 z^{-1}} \quad \wedge \quad \alpha_3 = \frac{\delta T_s \cdot G_m}{C_s + C_i} \quad \wedge \quad \beta_3 = \frac{C_i}{C_s + C_i} \tag{3.10}$$

The overall system transfer function can now be analyzed, given that the transfer function of the integrator is established. Fig. 3.7 illustrates the Z-domain block diagram of the $\Sigma\Delta$M shown at the begging of this chapter, incorporating a one-bit quantizer, as implemented by the quasi-passive modulator. The one-bit ADC is present at the output, modeled by a summing element where quantization noise $E(z)$ is injected, assuming ideal quantization. Quantization noise is also referred to as quantization error, as it represents the inherent error between the input analog signal and the output digital representation.

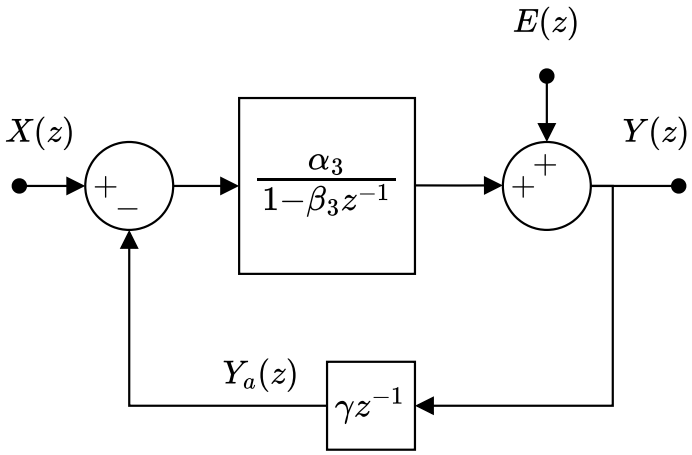


Figure 3.7: Block Diagram of a 1st-order ΣΔM.

Considering the output of block diagram, $Y(z)$ represents the summing of $E(z)$ and the integrator output $I(z)$, as expressed in (3.11).

$$Y(z)=I(z)+E(z) \tag{3.11}$$

Further, it is important to note that the quantized output $Y(z)$ undergoes digital-to-analog conversion within the feedback loop, resulting in an analog representation $Y_a(z)$ and that this process is controlled by a gain factor γ, which indicates its accuracy. The integrator output $I(z)$ can then be expressed in terms of $X(z)$, $Y(z)$, and $H_{qp}(z)$ as shown in (3.12).

$$I(z)=(X(z)-Y(z)\cdot\gamma z^{-1})\cdot H_{qp}(z) \tag{3.12}$$

By replacing the expression for $I(z)$ from (3.12) into (3.11), the overall transfer function of the system can be derived, resulting in (3.13). After some manipulation, this result simplifies to (3.14).

$$Y(z)=X(z)\cdot H_{qp}(z)-Y(z)\cdot H_{qp}(z)\cdot\gamma z^{-1}+E(z) \tag{3.13}$$

$$Y(z)=X(z)\cdot\frac{H_{qp}(z)}{1+H_{qp}(z)\cdot\gamma z^{-1}}+E(z)\cdot\frac{1}{1+H_{qp}(z)\cdot\gamma z^{-1}} \tag{3.14}$$

Replacing the expression from (3.10) into (3.14) produces the final result that contains all the variables, as seen in (3.15). The parameters α_3 and β_3 are defined as specified in (3.10).

$$Y(z)=X(z)\cdot\frac{\alpha_3}{1-(\alpha_3\gamma-\beta_3)z^{-1}}+E(z)\cdot\frac{1-\beta_3 z^{-1}}{1-(\alpha_3\gamma-\beta_3)z^{-1}} \tag{3.15}$$

From (3.15), two transfer functions can be derived, the signal transfer function (STF) and the noise transfer function (NTF), as seen in (3.16).

$$\mathrm{STF}(z)=\frac{\alpha_3}{1-(\alpha_3\gamma-\beta_3)z^{-1}} \quad \wedge \quad \mathrm{NTF}(z)=\frac{1-\beta_3 z^{-1}}{1-(\alpha_3\gamma-\beta_3)z^{-1}} \tag{3.16}$$

In the ideal case $\alpha_3=\beta_3=\gamma=1$, $\mathrm{STF}(z)=1$ and $\mathrm{NTF}(z)=(1-z^{-1})$. The output consists of the input signal combined with the quantization noise, which is shaped by a first-order Z-domain differentiator or high-pass filter [7]. For the non-ideal case, the dependence of STF on α_3 demonstrates that the input signal can be amplified without the requirement for OPAMPs [33]. Additionally, γ does not significantly affect the circuit, as long as $\alpha_3\gamma-\beta_3=0$. Evaluating the condition where $\alpha_3\gamma$ is equal to β_3 leads to the expression $\gamma=\frac{C_i}{\delta T_s\cdot G_m}$. Although the original value of γ is unknown, this expression identifies the value that results in optimal performance of the $\Sigma\Delta$M. From (3.10), it is also known that β_3 is always less than 1, which causes charge loss, as similarly discussed in Section 3.1.1. This loss highlights the need to control the ratio C_s/C_i when the capacitors are connected, as C_i must be significantly larger for C_s to be negligible and $\beta_3\approx 1$. Furthermore, C_s cannot be too small, as this would reduce the operating range for the C&H in current mode, as explained in Section 3.1.2. The proposed solution involves using a capacitor with variable capacitance, a MOSCAP, which allows C_s to be relatively large during sampling while minimizing capacitance during integration to reduce charge loss [28].

3.2 Building Blocks

The building blocks of the reference $\Sigma\Delta$M are examined to evaluate their contributions to the overall functionality of the system. This section analyzes the core elements of the system's architecture: the g_m cell, the bootstrapped switch, the MOSCAPs, and the StrongARM comparator. The area estimations are based on the original floorplan, while details regarding the bootstrapped switch and the comparator are derived from additional correspondence with the quasi-passive $\Sigma\Delta$M authors [28].

3.2.1 Transconductance Cell

The g_m cell is a crucial component of the reference $\Sigma\Delta$M [28]. As the front-end component of the circuit, it is the primary source of noise. The g_m cell uses an inverting amplifier which is a circuit widely used in both analog and digital circuits [34–37]. The schematic of the implemented circuit is shown in Fig. 3.8 [37]. The g_m cell continuously converts the input voltage to an output current, with a variable gain controlled by the dimensions of the transistors and the number of cells used in parallel.

A single side of the circuit is modeled as a one-input, one-output inverter-based amplifier. Therefore, only the left side of the circuit is considered to simplify the analysis. A further simplification involves analyzing only the N-type MOS (NMOS) portion of the circuit, given its complementary architecture. The analysis begins with the transistor connected to the common-mode feedback (CMFB) N_3, which stabilizes the output common-mode voltage. Together with the two sensing resistors and its complementary P-type MOS (PMOS), this transistor is biased in

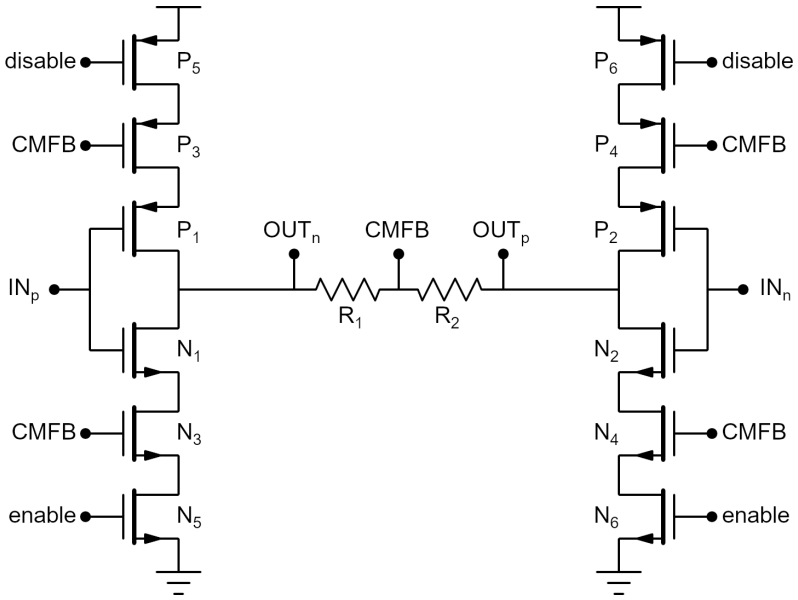


Figure 3.8: Reference g_m Cell Circuit Schematic.

the triode region. Therefore, N_3 can be modeled as a resistor, with its on-resistance determined by (3.17) [38]. In this context, μ represents the mobility of charge carriers, C_{ox} denotes the gate oxide capacitance per unit area, the aspect ratio $\frac{W}{L}$ indicates the width-to-length ratio of the transistor, and $|V_{GS}|-|V_{th}|$ refers to the overdrive voltage, which is the difference between the gate-source voltage and the threshold voltage. The operation of N_5 and its complementary counterpart, responsible for turning the g_m cell on and off, follows similar reasoning. The total degenerated resistance is equal to the series combination of these two on-resistances, referred to as R_S.

$$R_{on} = \frac{1}{\mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (|V_{GS}| - |V_{th}|)} \tag{3.17}$$

The g_m of the transistor N_1 is calculated as shown in (3.18). However, due to source degeneration, the circuit transconductance value is not determined solely by N_1. By analyzing the circuit expressions, the resulting transconductance is derived as shown in (3.19), incorporating the transconductance of N_1 and the on-resistances of the degenerated transistors, without accounting for the body effect of N_1 [38]. The total transconductance of the circuit is the sum of the NMOS and PMOS transconductance components, multiplied by 2 due to the differential architecture, as shown in (3.20) [38].

$$g_m = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (|V_{GS}| - |V_{th}|) = \sqrt{2\mu \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} \tag{3.18}$$

$$g'_m = \frac{g_m}{1 + g_m \cdot R_S} \tag{3.19}$$

$$G_m = 2 \cdot (g'_{m_n} + g'_{m_p}) \tag{3.20}$$

By increasing G_m, the g_m cell current output becomes more dependent on the input voltage signal, improving the circuit linearity. However, this gain is constrained by R_S. At low current levels $\frac{1}{g_m} >> R_S$, and hence $g'_m \approx g_m$. As the overdrive and therefore g_m increase, g'_m approaches $\frac{1}{R_S}$ [38].

A challenge in the CMFB arises because R_1 and R_2 must be much larger than the amplifier's output impedance to avoid reducing the open-loop gain. Large resistors, however, occupy significant area and suffer from parasitic capacitance to the substrate. Nonetheless, this does not pose a significant issue since the gain is not critical for the g_m cell, provided it is not extremely low ($A_0 << 1$) and ensuring the integrator operates in current mode, as discussed in Section 3.1.2. The sensitivity can be increased by reducing the resistance values, although this also increases the charge leakage through the gate of the CMFB transistors. Additionally, the overall circuit has two significant limitations [38]. First, the bias current of the circuit is highly dependent on process, voltage, and temperature (PVT) variations. Specifically, changes in supply voltage or threshold voltages lead to corresponding changes in the drain currents. Second, the circuit exhibits poor power supply rejection, as it amplifies variations in the supply voltage. However, this document will not address these issues, as the reference design has substantial potential for performance improvement.

The factors discussed throughout this subsection lead to the size values listed in Tab. 3.1. Both NMOS and PMOS transistors are implemented with a channel length of $500\,\mathrm{nm}$ to achieve high output impedance and low $1/f$ noise [37]. The resistors R_1 and R_2 are set as $50\,\mathrm{k\Omega}$.

Table 3.1: Baseline g_m Cell Transistors Dimensions.

Transistors	$P_{1,2}$	$P_{3,4}$	$P_{5,6}$	$N_{1,2}$	$N_{3,4}$	$N_{5,6}$
Width [µm]	5	2	2	2	0.5	0.25
Length [µm]	0.5	0.5	0.5	0.5	0.5	0.5

Certain parameters of the g_m cell, including power consumption and area, are not fully known. However, the area can be estimated [28]. The performance metrics are summarized in Tab. 3.2, which will be used for comparison purposes later in this study.

Table 3.2: Baseline g_m Cell Performance Metrics.

Area [μm^2]	G_m [µS]
40	23

3.2.2 Bootstrapped Switch

Conventional switches, such as NMOS and PMOS transistors, or transmission gates, exhibit varying on-resistance depending on the input voltage. This dependence introduces distortion, particularly in circuit nodes experiencing significant voltage swings, making them unsuitable for all ADC nodes. Bootstrapping is a method used to reduce on-resistance variation by keeping a constant gate-source voltage independent of the input voltage. This technique is achieved through a capacitor connected between the gate and source, which functions like a battery. As the input voltage changes, the gate and source voltages change proportionally, minimizing distortion from the switch.

The schematic of a bootstrapped switch circuit is shown in Fig. 3.9 [39]. The challenge with these devices lies in their size due to the associated capacitor. The capacitor C_b must be large enough to prevent significant voltage loss. To ensure that C_b fully charges to the supply voltage during the hold mode, the series combination of P_1, C_b, and N_1 must exhibit a time constant of less than half the clock period. All transistors in the circuit are sized with a width of $160\,\mathrm{nm}$ and a length of $120\,\mathrm{nm}$ to optimize area and speed. The capacitor C_b is sized at $20\,\mathrm{fF}$ to store sufficient charge during the clock cycle and maintain the bootstrapping effect.

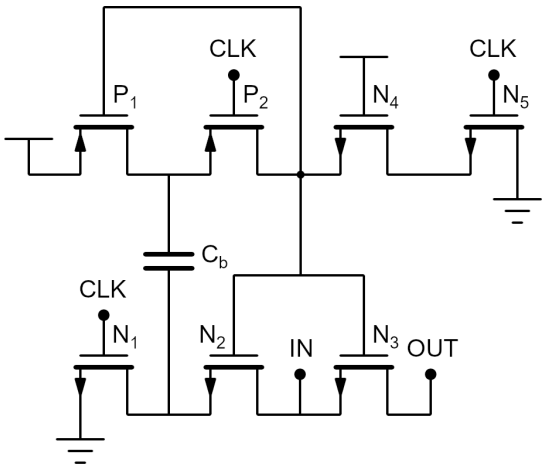


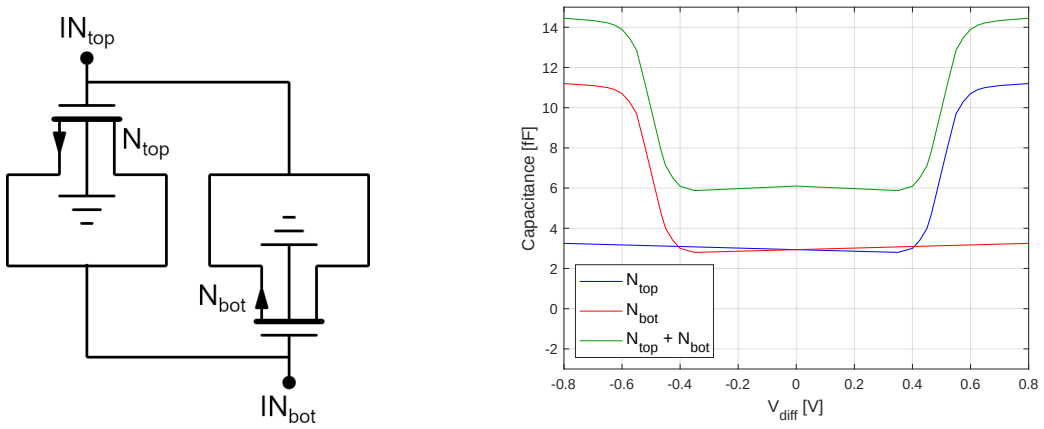
Figure 3.9: Bootstrapped Switch Circuit Schematic.

Contrary to the previous component, it is not possible to estimate key performance parameters, such as power consumption or area, for this building block. However, this limitation does not pose a significant issue, as these parameters can be evaluated during later stages of the study.

3.2.3 MOSCAPs

A MOSCAP comprises a metal-oxide semiconductor (MOS) transistor with shorted source and drain terminals, functioning as a capacitor that stores charge between the gate and bulk terminals. The MOSCAPs generate ideally no noise and operate at high sampling rates with minimal static power consumption. The primary advantage of using MOSCAPs over traditional linear capacitors lies in their variable capacitance, which can be utilized to amplify signals [40–43] and, in the case of the reference $\Sigma\Delta$M, to reduce charge leakage [28].

The gate-bulk capacitance C_{gb} of a MOSCAP depends on the voltage at which the source-drain terminal is connected. When the source-drain terminal is grounded, and the gate-source voltage is sufficiently high, the transistor operates in the strong inversion region, forming a large capacitor with a value C_{ox}. If there is a high potential at the source-drain terminal, the transistor enters the depletion region and prevents the formation of the inversion layer. In this state, C_{gb} is expressed by the series connection of the capacitance of the depletion region C_{dep}, and C_{ox}. The chosen topology, shown in Fig. 3.10(a), consists of two parallel complementary MOSCAPs [44]. Fig. 3.10(b) illustrates the capacitance curves for varying voltages, demonstrating that the two capacitance curves are complementary, with V_{diff} representing the differential voltage between the two input nodes.



(a) Circuit Schematic

(b) Capacitance vs. Input Voltage Example

Figure 3.10: MOSCAP Complementary Topology.

There are three MOSCAPs to be dimensioned in the reference $\Sigma\Delta$M: the sampling MOSCAP C_s, the DAC MOSCAP C_{DAC}, and the integrating MOSCAP C_i. The width W of C_s and C_i is set to the minimum size of $160\,\mathrm{nm}$ in the $130\,\mathrm{nm}$ technology, ensuring a low $\frac{W}{L}$. This low ratio enhances the capacitance difference exhibited by the MOSCAP in the two operating regions, as later detailed in Section 4.1.3 [28, 44].

Three key factors must be considered when sizing C_s. First, the capacitance must be high enough to prevent the integrator from saturating or switching to voltage mode, maximizing charge linearity, as discussed in Section 3.1.2. Second, a common mode voltage greater than $0.5\,\mathrm{V}$ at the output of the g_m cell is necessary to bias the MOSCAPs at high capacitance mode. Finally, the output differential voltage must be large to achieve a wide dynamic range within the $\Sigma\Delta$M. With these considerations, C_s is set to $300\,\mathrm{fF}$, implemented with 12 MOSCAPs in parallel ($m=12$) with a length L of $12\,\mu\mathrm{m}$ to accumulate the charge generated by the g_m cell.

The capacitance of C_{DAC} must be significantly smaller than C_s to prevent saturation of the $\Sigma\Delta$M, as C_{DAC} is connected to the supply voltage ($1.2\,\mathrm{V}$) or ground. The dimensioning is based on the charge transferred to C_s during each iteration. Using then $Q=C\times V$, the capacitance C_{DAC} can be estimated. The length of the DAC MOSCAP transistors is set to $4.3\,\mu\mathrm{m}$, with $m=2$, yielding a capacitance of $16.1\,\mathrm{fF}$.

The integrating MOSCAPs are critical in reducing charge leakage between all capacitors. To minimize leakage when disconnecting C_s and C_{DAC} from C_i, the ratios C_s/C_i and C_{DAC}/C_i should be minimized, as discussed in Section 3.1.3. While the use of MOSCAPs in C_s and C_{DAC} helps to reduce leakage, further improvement can be achieved by making C_i significantly larger than C_s and C_{DAC}. However, if C_i is too large, the integration voltage becomes too small relative to the comparator noise, leading to errors and reduced performance. The dimensions of the C_i MOSCAP transistors are set to $W=L=20\,\mu\mathrm{m}$ and $m=1$, resulting in a capacitance of $4.61\,\mathrm{pF}$.

In a similar manner to the g_m cell, the total area of the MOSCAPs is not directly available but can be approximated [28]. The main performance metrics are detailed in Tab. 3.3.

Table 3.3: Baseline MOSCAPs Performance Metrics.

Area [μm^2]	C_s [fF]	C_{DAC} [fF]	C_i [fF]
1440	300	16.1	4610

3.2.4 Comparator

The StrongARM latch comparator is a commonly utilized topology characterized by very low static power consumption, rail-to-rail outputs, and minimal input-referred offset [45]. As depicted in Fig. 3.11, the comparator consists of a clocked differential pair of transistors, N_1 and N_4, and two cross-coupled pairs that form a latch, N_2 with N_3 and P_3 with P_4. Additionally, it incorporates four switches, P_1, P_2, P_5, and P_6, which connect to the supply voltage when the reset signal is high. When the reset signal is low, the outputs adjust based on the input voltage difference. The StrongARM latch comparator is optimized using the NSGA-II algorithm, resulting in an input-referred noise of $0.296\,\mathrm{mV}$ [46]. However, since it was not explicitly designed for the reference $\Sigma\Delta$M, there is potential for enhancing its power efficiency.

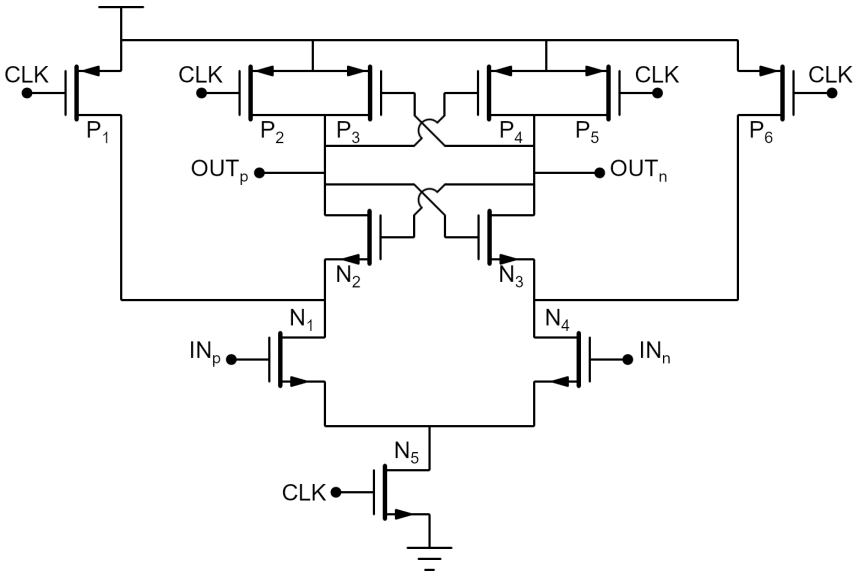


Figure 3.11: Reference Comparator Circuit Schematic.

Similarly to the bootstrapped switch, limited information is available regarding key performance parameters such as power consumption, area, or the dimensioning of this building block. However, some of these parameters can be derived [28]. The performance metrics of the StrongARM comparator are presented in Tab. 3.4.

Table 3.4: Baseline Comparator Performance Metrics.

Area [μm^2]	V_n [mV]	**Compare Time** [ns]	**Reset Time** [ns]
400	0.296	0.83	0.21

3.3 Global Overview

The top-level architecture of the quasi-passive $\Sigma\Delta$M is illustrated in Fig. 3.12. The MOSCAPs are depicted as variable capacitors. The bootstrapped switches correspond to switches S_1 to S_6, while switches S_7 to S_{12} are implemented as single transistor switches. The g_m cell and comparator are each represented using their respective symbols.

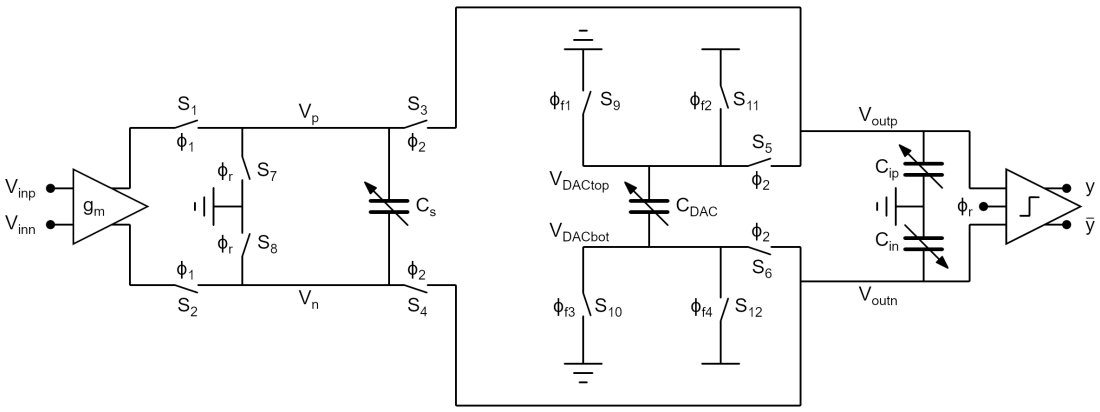


Figure 3.12: Top-Level $\Sigma\Delta$M Circuit Schematic.

The ϕ_{fn} clocks shown in Fig. 3.12 represent the feedback control clocks, which are determined by the functions outlined in Tab. 3.5. A reset signal ϕ_r is applied between each cycle to fully discharge the sampling capacitors and activate the comparator, allowing it to produce a digital word modulated by the analog input signal.

Table 3.5: Functions for the Feedback Control Clocks.

$\boldsymbol{\phi_{f1}}$	$\boldsymbol{\phi_{f2}}$	$\boldsymbol{\phi_{f3}}$	$\boldsymbol{\phi_{f4}}$
$y \wedge \phi_1$	$y \vee \bar{\phi}_1$	$\bar{y} \wedge \phi_1$	$\bar{y} \vee \bar{\phi}_1$

Fig. 3.13 illustrates the differential operation of the modulator by presenting the circuit waveforms across three clock cycles [28]. Initially, input voltages are converted into currents via the g_m cell. These currents are then transferred to the sampling MOSCAPs. The charge stored in C_s is subsequently transferred to the integrating capacitors. After the charge transfer, the latched comparator measures the voltages across both C_i capacitors. Based on the comparator's output, denoted as y, feedback is applied by the DAC capacitors to either the positive or negative reference, as indicated by V_{DACtop} and V_{DACbot}. The DAC capacitors are charged during the sampling process. The charge in both C_{DAC} and C_s is transferred simultaneously to the integrating capacitors, and the comparator measures the resulting voltages to generate a new output, repeating the cycle.

Finally, the $\Sigma\Delta$M performance metrics are presented in Tab. 3.6. The value presented for the area is based on a floorplan rather than an actual layout implementation. A tape-out run in TSMC $65\,\mathrm{nm}$ technology motivates the porting of the presented circuit and subsequent layout implementation for fabrication as an opportunity to verify the quasi-passive $\Sigma\Delta$M architecture in silicon and, thereby, add a practical component to the thesis. The next chapter details this porting process of the circuit.

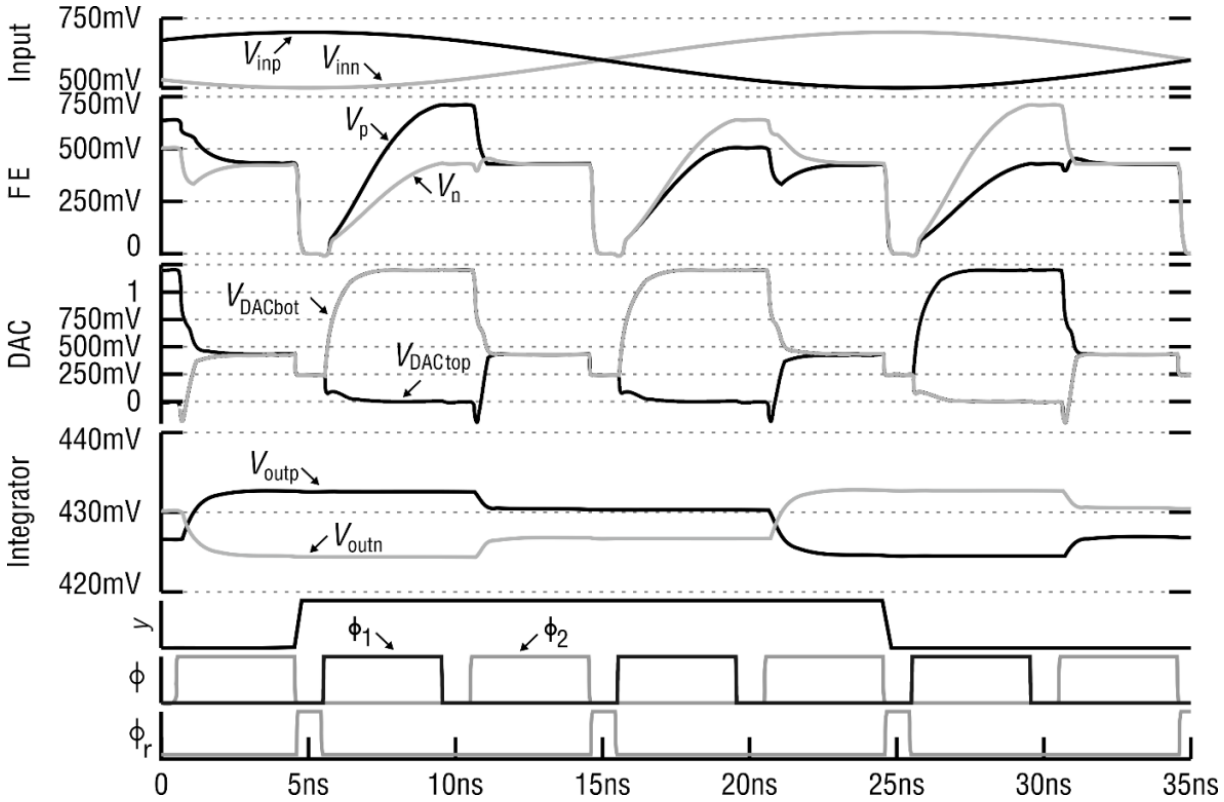


Figure 3.13: ΣΔM Circuit Waveforms [28].

Table 3.6: Baseline ΣΔM Performance Metrics.

Technology [nm]	130
Area [μm^2]	2400
Supply Voltage [V]	1.2
Samp. Frequency [MHz]	100
Bandwidth [kHz]	390.63
Front-End ENOB [bit]	12.03
ΣΔM ENOB [bit]	8.23
Power Consumption [μW]	80
FoM$_2$ [$fJ/conv-step$]	339.7
FoM$_3$ [$fJ \cdot mm^2/conv-step$]	0.82

Chapter 4

Circuit Porting Procedure

The $\Sigma\Delta$M used as an initial reference for the proposed architecture lacks a complete layout but provides a floorplan that approximates the placement of its functional blocks, enabling area estimations for these building blocks, as presented in Section 3.2. Upon establishing the behavior and theoretical foundation of each building block, and prior to optimization, the primary objective is to achieve an operational design from which the layout can be developed to verify the quasi-passive $\Sigma\Delta$M architecture in silicon. A preliminary fabrication opportunity supports this development, adding an extra practical component to the thesis, although it imposes a tight tape-out schedule. Due to these time constraints, the porting process is conducted as directly and efficiently as possible, maintaining design dimensions where feasible. This chapter details the process of porting the circuit from UMC $130\,\mathrm{nm}$ to TSMC $65\,\mathrm{nm}$ technology, with a focus on key performance metrics analysis rather than comprehensive functional comparisons.

4.1 Design Adaptations

The first modification in the original circuit is adjusting the sampling frequency. The reference $\Sigma\Delta$M is designed for a sampling frequency of $100\,\mathrm{MHz}$ with an OSR of 128, resulting in a bandwidth of $390.625\,\mathrm{kHz}$. Given that the bandwidth requirements for the application described in Chapter 1 fall within the range of $50\,\mathrm{kHz}$, a sampling frequency of $15\,\mathrm{MHz}$ is selected. With an OSR of 128, this yields a bandwidth of $58593.75\,\mathrm{Hz}$. This adjustment is expected to reduce power consumption at least 6.7 times due to its linear frequency dependence [25].

The reference $\Sigma\Delta$M Cadence® Virtuoso library is organized as part of the design adaptation process, including schematics and test benches. Many components used in the reference design are ideal blocks (e.g., g_m cell resistors and bootstrapped switch capacitor) since this $\Sigma\Delta$M is not implemented in layout. Furthermore, the porting process requires removing global nets and replacing ideal blocks within the building block schematics. This procedure introduces the initial challenge of selecting suitable TSMC $65\,\mathrm{nm}$ technology capacitors and resistors. The following subsections address the modifications to each building block and the control logic, outlining the key challenges during the porting process.

4.1.1 Transconductance Cell

As described in Section 3.2.1, the g_m cell consists of 12 transistors and 2 resistors in its implementation. Among these components, the resistor implementation presents the primary challenge in the porting process. Resistors can be fabricated in CMOS technology using doped polysilicon (Poly) and three types of diffusions: N+, P+, and N-Well. The N+ and P+ diffusions serve as the drain and source for NMOS and PMOS transistors, respectively, while the N-Well functions as the body of a PMOS transistor. N+ and P+ diffusions exhibit shallow junctions with lower sheet resistance, making them suitable for low-value resistors. In contrast, the N-Well has a deeper junction, which is advantageous for high-value resistors, mainly when the absolute value or temperature dependence is less critical. The salicide process is employed to create metal silicide contacts, which reduces the resistance of these devices and decreases temperature dependence from the introduction of metal. Doped Poly is commonly used as a precise analog resistor element with low-temperature sensitivity, and these resistors exhibit compactness due to the high resistance per square or $\Omega/\square$ [47, 48].

Given the objective of minimizing area, a Poly resistor is selected. Specifically, a P+ Poly resistor without salicide from TSMC $65\,\mathrm{nm}$ technology is used, which has a sheet resistance of $690.023\,\Omega/\square$. The width is set to $400\,\mathrm{nm}$ to achieve a compact design. To create the necessary $50\,\mathrm{k}\Omega$ resistor, a length of $26.31\,\mu\mathrm{m}$ is required. Since two resistors with dimensions of $26.31\,\mu\mathrm{m}$ by $400\,\mathrm{nm}$ would result in area inefficiency, the number of segments is kept at three. This segmentation means that the total resistor is a series connection of three resistors, each measuring $8.77\,\mu\mathrm{m}$ by $400\,\mathrm{nm}$, yielding a total size of $9.45\,\mu\mathrm{m}$ by $1.7\,\mu\mathrm{m}$, including metal contacts. The transistors in the g_m cell are the same size as presented in Section 3.2.

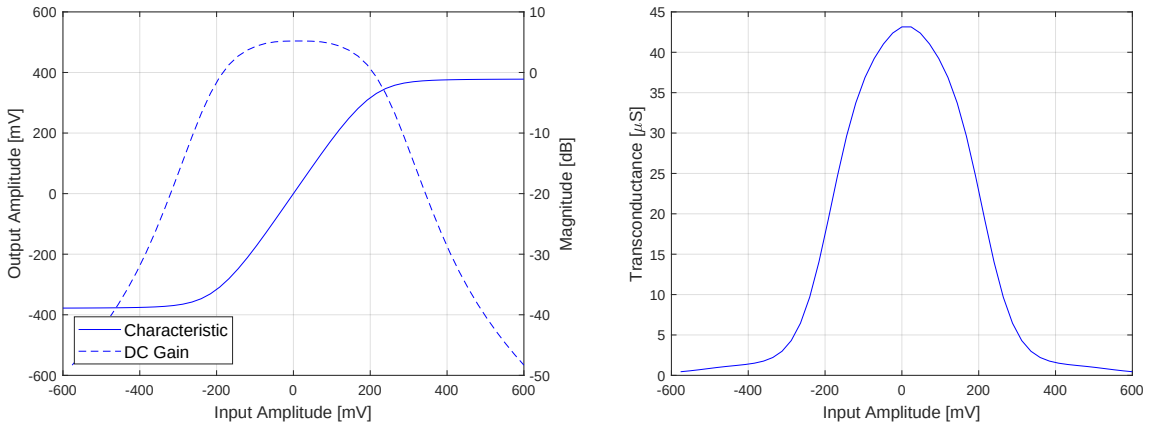
Fig. 4.1 shows the DC characteristics of the g_m cell. Ideally, the output voltage range, or dynamic range, should be maximized while maintaining a linear relationship between the input and output over a wide range of input voltages. This implementation achieves a linear gain over an input voltage range of $329\,\mathrm{mV}$, which covers only $27\,\%$ of the total supply voltage range, with a dynamic range of $756\,\mathrm{mV}$. Additionally, tests on the g_m cell reveal other performance metrics, summarized in Tab. 4.1, with a maximum measured G_m of $43.14\,\mu\mathrm{S}$, coming as an expected result [49]. These values are obtained using the appropriate test benches [34, 35].

Table 4.1: 1st Version g_m Cell Performance Metrics.

A_0 [dB]	**Bandwidth** [MHz]	**Dynamic Range** [mV]	G_m [µS]	V_n [mV]
5.2	6.4	756	43.14	0.138

4.1.2 Bootstrapped Switch

As outlined in Section 3.2.2, the bootstrapped switches comprise 7 transistors and 1 capacitor. Similar to the g_m cell, the implementation of the capacitor poses the main challenge in the porting process. Capacitors typically occupy substantial chip space in circuit layouts, making efficient area utilization a significant factor in CMOS IC design. The three common types of capacitors used are metal-insulator-metal (MIM), metal-oxide-metal (MOM), and MOS capacitors, each possessing distinct characteristics.



(a) DC Transfer Function and Gain

(b) Transconductance vs. Input Voltage

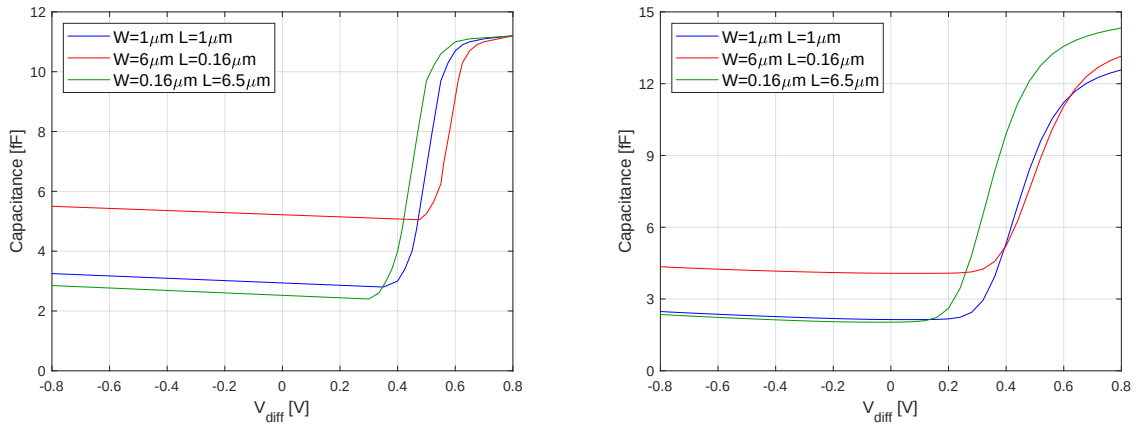
Figure 4.1: 1st Version g_m Cell DC Characteristics.

The bootstrapped switch capacitor must exhibit linear behavior to avoid introducing distortion in the various stages of the $\Sigma\Delta$M [28]. For this reason, MOSCAPs are not considered due to their inherent non-linearity. MIM and MOM capacitors provide more reliable characteristics but come with lower capacitance densities. MOM capacitors typically require less silicon area compared to MIM capacitors for the same capacitance, mainly when more metal layers are employed. While MIM capacitors may offer advantages in specific processes, they require additional fabrication steps and masks, leading to higher production costs. On the other hand, MOM capacitors, constructed from existing metal interconnections, do not necessitate additional masks, simplifying integration and reducing manufacturing costs [50]. Due to their higher capacitance density and lower fabrication expenses, MOM capacitors are deemed more appropriate for the bootstrapped switch.

The transistors in the bootstrapped switch are kept close to the minimum size, with a width of $200\,\mathrm{nm}$ and a length of $60\,\mathrm{nm}$, to optimize both area efficiency and speed. The capacitor C_b is designed with a value of $20\,\mathrm{fF}$, corresponding to a MOM capacitor with dimensions of $3.8\,\mu\mathrm{m}$ by $9.6\,\mu\mathrm{m}$.

4.1.3 MOSCAPs

To compare the differences between UMC $130\,\mathrm{nm}$ and TSMC $65\,\mathrm{nm}$ technologies, a study on MOSCAPs with an area of $1\,\mu\mathrm{m}^2$ is conducted. The MOSCAP aspect ratio $\frac{W}{L}$ plays a significant role in shaping the $C(V)$ curve, as shown in Fig. 4.2 [44]. This characteristic is pertinent to the study, as it aids in understanding the differences associated with various sizing choices. Both Figs. 4.2(a) and 4.2(b) compare MOSCAPs with different $\frac{W}{L}$ but similar maximum capacitance. The results indicate that higher $\frac{W}{L}$ leads to an increase in the threshold voltage V_{th} of the MOSCAP. Additionally, it expands the low capacitance region and decreases the capacitance amplitude between the two operating zones. However, a larger $\frac{W}{L}$ also leads to increased parasitic capacitances. In contrast, a smaller $\frac{W}{L}$ narrows the region of reduced capacitance and exhibits less parasitic capacitance [44].



(a) UMC $130\,\mathrm{nm}$ Technology

(b) TSMC $65\,\mathrm{nm}$ Technology

Figure 4.2: Capacitance vs. Input Voltage for Different Aspect Ratios and Technologies.

Moreover, $\frac{W}{L}$ also affects frequency dependence, with simulations indicating that higher $\frac{W}{L}$ increase the input frequency threshold at which the maximum capacitance begins to decrease or be affected. For the $65\,\mathrm{nm}$ technology, the maximum capacitance is only impacted at an input frequency of $10\,\mathrm{GHz}$, compared to $100\,\mathrm{MHz}$ for the $130\,\mathrm{nm}$ technology [44].

From comparing Figs. 4.2(a) and 4.2(b), the differences between the two technologies are small but evident in two key areas. First, V_{th} is lower for the $65\,\mathrm{nm}$ technology at about $350\,\mathrm{mV}$, compared to $500\,\mathrm{mV}$ for the $130\,\mathrm{nm}$ technology. Second, the C_{ox} of the $65\,\mathrm{nm}$ technology is notably higher, with $65\,\mathrm{nm}$ MOSCAPs achieving roughly $20\,\%$ more capacitance for the same area compared to the $130\,\mathrm{nm}$ technology.

The required MOSCAPs C_s, C_{DAC}, and C_i can now be designed in the newer technology. The dimensions provided in Section 3.2 are adjusted to achieve original capacitances of $300\,\mathrm{fF}$, $16.1\,\mathrm{fF}$, and $4.61\,\mathrm{pF}$ for C_s, C_{DAC}, and C_i, respectively. For C_s, the sizing is carried with a width W of $160\,\mathrm{nm}$ and a length L of $10\,\mu\mathrm{m}$, implemented using 12 MOSCAPs in parallel ($m = 12$), resulting in a total capacitance of $280\,\mathrm{fF}$. The complementary MOSCAPs for C_{DAC} have a W of $160\,\mathrm{nm}$, L of $2.8\,\mu\mathrm{m}$, and $m = 2$, achieving a capacitance of $13.3\,\mathrm{fF}$. Lastly, C_i transistors are implemented with a width and length of $12\,\mu\mathrm{m}$ and $m = 2$, resulting in a total capacitance of $3.66\,\mathrm{pF}$. The discrepancy in C_i capacitance value is explained from the optimization on its dimensions to maximize the ENOB.

4.1.4 Comparator

The comparator discussed in Section 3.2.4 exhibits limitations, particularly its lack of driving capability. A collaboration with João Silva from INESC-ID addresses these limitations, providing a more robust design that incorporates inverter logic gates at the input clock and output nodes [51]. This design is optimized using the NSGA-II algorithm [52]. The improved implementation performs input comparison in $300\,\mathrm{ps}$, which is

three times faster than the comparator described in Section 3.2.4, while also enhancing robustness without compromising the input-referenced noise. Fig. 4.3 shows the comparator, which includes an additional reset transistor and three inverter logic gates.

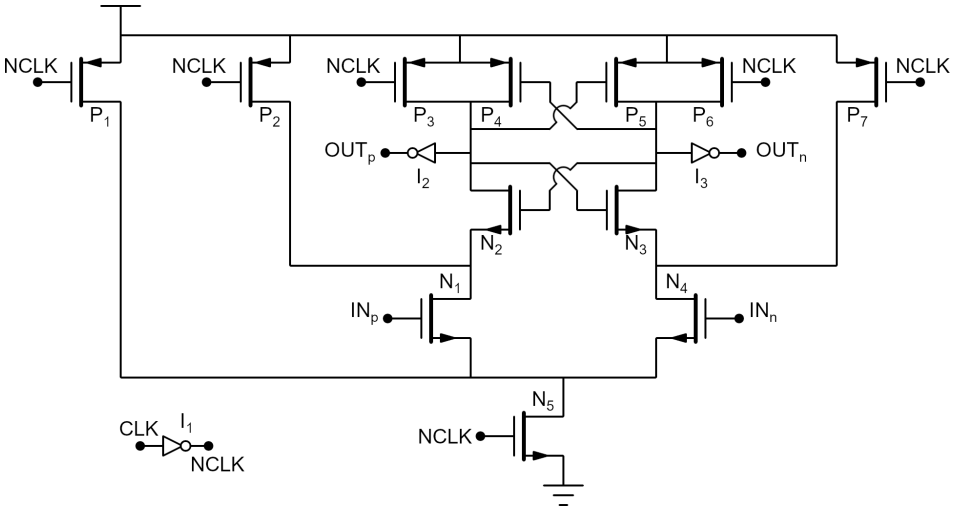


Figure 4.3: 1st Version Comparator Circuit Schematic.

The sizing values are shown in Tab. 4.2. Furthermore, the performance metrics of the comparator are summarized in Tab. 4.3.

Table 4.2: 1st Version Comparator Transistors Dimensions.

Transistors	$P_{1,2,3,6,7}$	$P_{4,5}$	$N_{1,4}$	$N_{2,3}$	N_5	P_{I1}	N_{I1}	$P_{I2,I3}$	$N_{I2,I3}$
Width [µm]	0.33	0.13	4.75	0.59	6	2	1.2	2.84	0.54
Length [µm]	0.06	0.065	0.065	0.065	0.065	0.06	0.06	0.06	0.06

Table 4.3: 1st Version Comparator Performance Metrics.

V_n [mV]	**Compare Time** [ns]	**Reset Time** [ns]
0.308	0.3	0.16

4.1.5 Control Logic

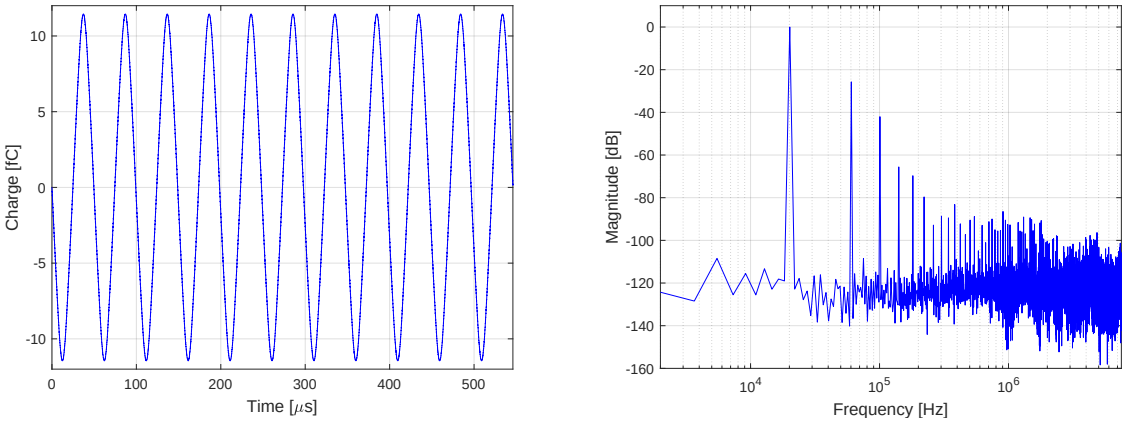
The reference ΣΔM requires three non-overlapping clocks, ϕ_1, ϕ_2, and ϕ_r, in order to work, as stated in Section 3.3. These clocks are kept external to simplify the porting process. However, the feedback loop also requires control clocks, which are logical combinations of ϕ_1 and the comparator output y, as detailed in Tab. 4.4. To achieve this, 6 inverters, 2 Not ANDs (NANDs), and 2 Not ORs (NORs) logic gates from the TSMC $65\,\mathrm{nm}$ analog library are used. For these logic gates, NMOS transistors have a length of $60\,\mathrm{nm}$ and a width of $150\,\mathrm{nm}$, while PMOS transistors have a length of $60\,\mathrm{nm}$ and a width of $500\,\mathrm{nm}$. This sizing ensures a $1{:}3.33$ proportion in aspect ratio, which is necessary for electron mobility compensation and to achieve a matched logic cell [30, 53].

Table 4.4: Functions for the Feedback Control Clocks.

ϕ_{f1}	ϕ_{f2}	ϕ_{f3}	ϕ_{f4}
$y \wedge \phi_1$	$y \vee \bar{\phi}_1$	$\bar{y} \wedge \phi_1$	$\bar{y} \vee \bar{\phi}_1$

4.2 Pre-Layout Simulations

The circuit test bench consists of a transient simulation with a differential input signal having an amplitude of $200\,\mathrm{mV}$ at a frequency of $20141.6\,\mathrm{Hz}$, selected to achieve coherent sampling, and a sampling frequency of $15\,\mathrm{MHz}$, under typical conditions. This sinusoidal signal is added to a DC voltage, set to half of the supply voltage, $600\,\mathrm{mV}$, properly biasing the g_m cell. The charge linearity of the modulator front-end is first measured using a Verilog-A block [54], which calculates the charge transferred to the sampling MOSCAPs during each clock period. The output charge, presented in Fig. 4.4, is sampled at 8192 points to ensure coherent sampling, preventing resolution degradation due to spectral leakage [55]. The discrete Fourier transform (DFT) of the charge, along with all other signals analyzed in this section, is computed using a Python3 script from INESC-ID [54].



(a) Differential Charge Sine Signal

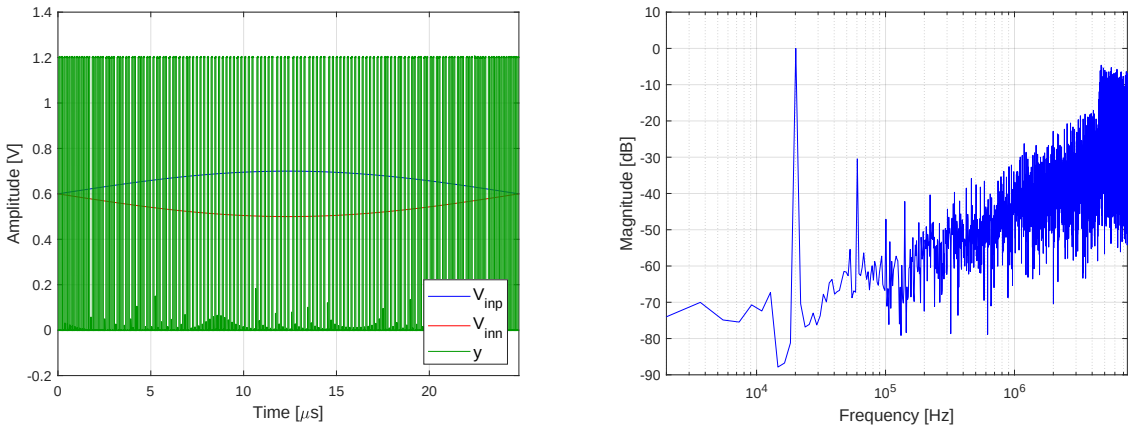
(b) Respective DFT

Figure 4.4: Front-End Transient Simulation.

The sinusoidal waveform in Fig. 4.4(a) illustrates the differential charge of the $\Sigma\Delta$M front-end, with an amplitude of $11.45\,\mathrm{fC}$. This waveform reflects the expected performance of the complete $\Sigma\Delta$M, as the charge linearity directly correlates with the modulator's voltage output, as studied in Section 3.1.3. The front-end demonstrates an ENOB of $3.97\,\mathrm{bit}$ due to aliasing in the odd harmonics, confirmed by the DFT in Fig. 4.4(b). When the harmonics are excluded, the front-end achieves an ENOB of $14.91\,\mathrm{bit}$, indicating a low noise floor. This resolution inefficiency is attributed to saturation in the g_m cell, which causes aliasing. The next version of the $\Sigma\Delta$M addresses this issue.

For the complete $\Sigma\Delta$M test bench, an ideal output capacitor of $100\,\mathrm{fF}$ is used to simulate the input capacitance of a future decimator and evaluate whether the StrongARM comparator can drive such load. The

output voltage node y of the $\Sigma\Delta$M is used to assess the resolution by computing the DFT of the waveform, utilizing again 8192 points to maintain coherent sampling. Fig. 4.5 presents half a period of the input voltages to illustrate the modulation effect, along with the modulated output bit stream and the associated DFT. The output y is a binary waveform with a frequency of $15\,\mathrm{MHz}$, modulated by the input differential voltage. In Fig. 4.5(b), it is shown that the noise is shaped to higher frequencies, as discussed in Sections 2.4 and 3.1.3. In the complete implementation, the distortion by the odd harmonics is reduced due to feedback but remains present and requires further consideration in the next $\Sigma\Delta$M version. The ENOB obtained from the spectrum, assuming an OSR of 128, is $8.178\,\mathrm{bit}$, which closely matches with the original result of $8.230\,\mathrm{bit}$ [28]. This ENOB results from the particularly high third harmonic being filtered with an OSR of 128. With an OSR of 64, the third harmonic is not filtered, leading to an ENOB of $5.013\,\mathrm{bit}$, which is considered suboptimal. In addition to ENOB performance, power consumption is also analyzed.



(a) Input vs. Output Signals

(b) Output Signals DFT

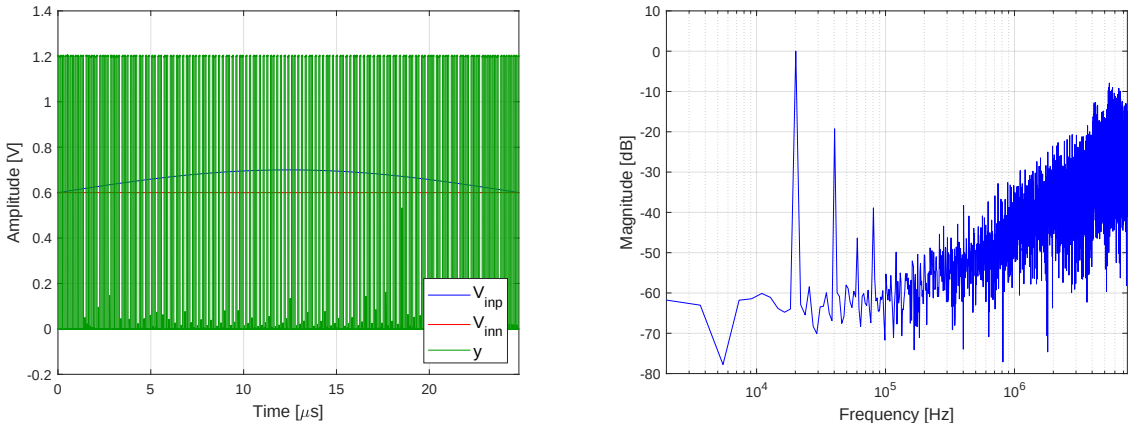
Figure 4.5: Complete $\Sigma\Delta$M Differential Transient Simulation.

The total power consumption of the complete $\Sigma\Delta$M measures $11.09\,\mu\mathrm{W}$. This result shows a power consumption reduction of 7.2 times compared to the values presented in Section 3.3. Tab. 4.5 presents the power consumption for each building block, showing that the g_m cell contributes the most at $64.5\,\%$ of the total power, followed by the comparator. It should be noted that the comparator's total power consumption is dependent on the output load, with the static power consumption being $0.95\,\mu\mathrm{W}$. This implementation of the comparator demonstrates a $25\,\%$ improvement in power consumption while being able to supply larger loads compared to the original version of the comparator discussed in Section 3.2.4.

Further, a test is conducted using only one input, effectively configuring the $\Sigma\Delta$M as a single-input system instead of differential. It is important to ensure that the unused input is still connected to half of the supply DC voltage to properly bias the g_m cell. The results from this test are shown in Fig. 4.6.

Table 4.5: Power Distribution for the 1st Version $\Sigma\Delta$M.

Building Block	**Power Consumption** [μW]	**Power Percentage** [%]
g_m Cell	7.156	64.5
Bootstrapped Switches	0.199	1.8
StrongARM Comparator	3.099	28.0
Control Logic	0.636	5.7



(a) Input vs. Output Signals

(b) Output Signals DFT

Figure 4.6: Complete $\Sigma\Delta$M Single-Input Transient Simulation.

The output bit stream maintains a modulated appearance, but the calculated DFT exhibits harmonics of second and third order, resulting in an ENOB of $2.883\,\mathrm{bit}$ for an OSR of 128. A fully differential modulator is expected to be free from second-order harmonic distortion [56], meaning that the distortion observed in Fig. 4.6(b) is attributed to using the $\Sigma\Delta$M in single-input mode. This limitation is also addressed in the next $\Sigma\Delta$M version. As previously mentioned, time constraints limited the number of simulations and the preparation for tape-out. As a result, corner simulations and Monte Carlo (MC) simulations are not performed for this version of the $\Sigma\Delta$M.

4.3 Layout Design

In the manufacturing process, the layout is a critical component of the design flow. The performance of a differential architecture is highly dependent on its layout, witch must be constructed symmetrically to preserve the advantages of this architecture [56]. Once the layout is completed, the design is validated through Design Rule Check (DRC) and Layout vs. Schematic (LVS) to ensure compliance with foundry specifications. Following this, Parasitic Extraction (PEX) is conducted to produce a parasitic netlist that captures the parasitic characteristics of the layout. The PEX netlist can then be simulated to verify every performance metric of the $\Sigma\Delta$M. These design principles result in the layout shown in Fig. 4.7. The various components are labeled, except the bootstrapped switches, represented by the six unlabeled groups of components. The layout dimensions are $27.4\,\mu\mathrm{m}$ by $63.3\,\mu\mathrm{m}$, leading to a total active area of $1735\,\mu\mathrm{m}^2$.

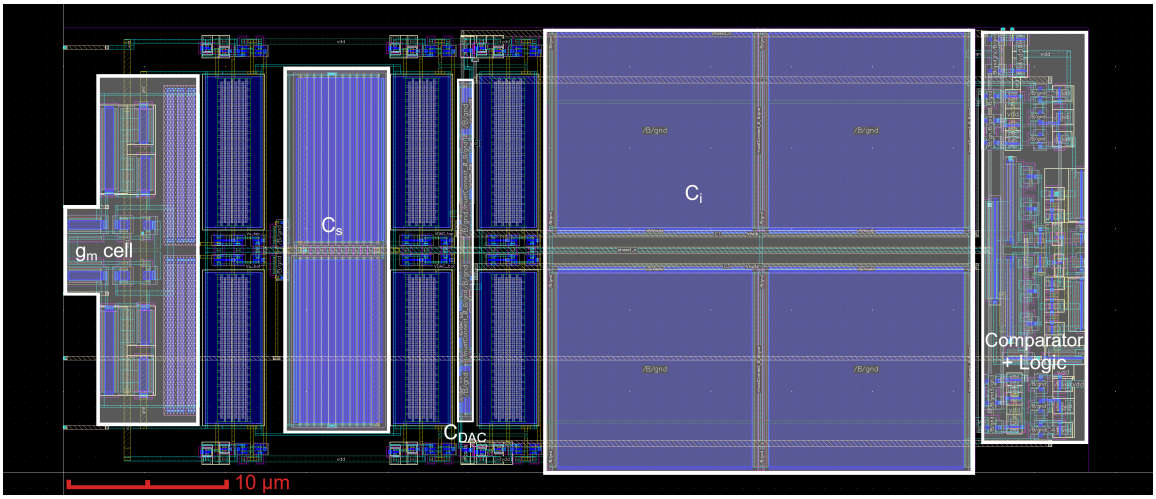


Figure 4.7: 1st Version ΣΔM Layout Implementation.

Moreover, as the tape-out is shared with another project, the pads are positioned on the available sides, as illustrated in Fig. 4.8. The pads used include electrostatic discharge (ESD) protection. The ΣΔM is highlighted with a white frame. It can be observed that the first version is already smaller than a pad. A yellow metal diffusion is also visible around the modulator. This metal layer 2 and the metal layer 1 beneath it form a capacitor between the supply voltage and ground, filtering supply voltage variations while using otherwise empty space for a practical purpose. This circuit, including the pads, measures $355\,\mu\mathrm{m}$ by $980\,\mu\mathrm{m}$, yielding a total area of $0.348\,\mathrm{mm}^2$.

At this stage, two comparisons are carried out. The first involves comparing the areas obtained by this initial version with the sizes reported in Section 3.2 [28]. This assessment utilizes the symbols $\searrow$ and $\nearrow$ to indicate decrease and increase, respectively. The second comparison focuses on the percentage of area occupied by each building block, providing insight into which block should be prioritized for optimization to reduce the overall area in the next version. Tab. 4.6 summarizes this data.

Table 4.6: Area Comparison and Distribution of the 1st Version ΣΔM.

Building Block	**Original Area** [$\mu\mathrm{m}^2$]	**1st Version Area** [$\mu\mathrm{m}^2$]	**Area Percentage** [%]
g_m Cell	40	169.2 (4.2× $\nearrow$)	9.8
MOSCAPs	1440	884.2 (1.6× $\searrow$)	51.0
Bootstrapped Switches	-	354.3	20.4
StrongARM Comparator	400	84.5 (4.7× $\searrow$)	4.9
Control Logic	400	67.3 (5.9× $\searrow$)	3.9
Complete ΣΔM	2400	1735 (1.38× $\searrow$)	100

The data presented in this section allows for several conclusions. Firstly, despite the circuit being ported directly with minimal changes, the total area is reduced by $27.7\,\%$. As expected, the MOSCAPs are the largest contributors to the total chip area. The bootstrapped switches follow, a factor not considered in the initially proposed circuit [28]. For the g_m cell, $25\,\%$ of its area is occupied by the sensing resistors, indicating that the resistors' size should be reconsidered. Finally, as indicated in Tab. 4.6, approximately $14\,\%$ of the area remains unoccupied or is used for interconnect purposes. This percentage should be minimized to achieve better compactness.

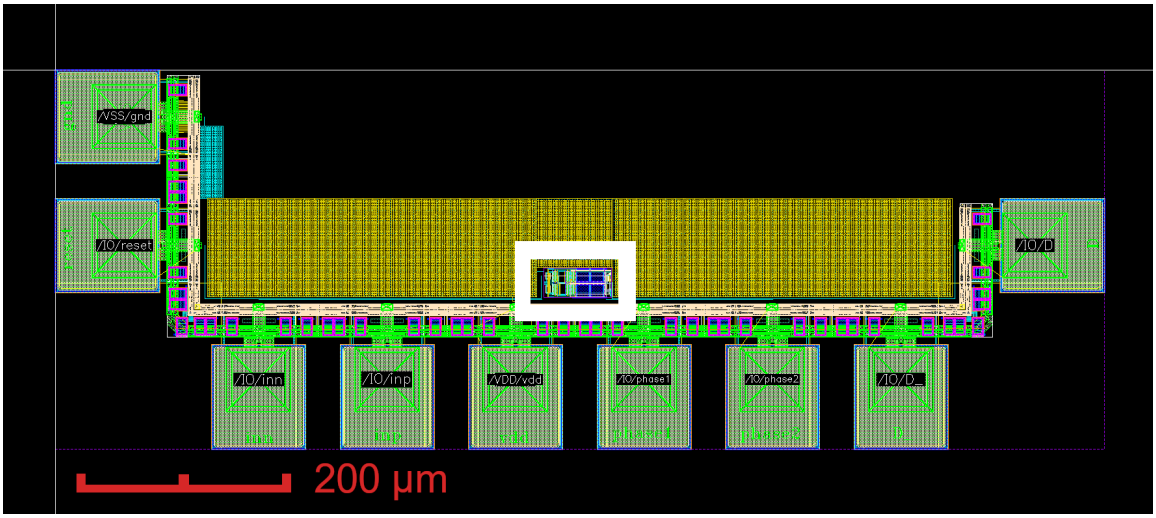


Figure 4.8: 1st Version $\Sigma\Delta$M Layout Implementation with Pads.

4.4 Post-Layout Results

The parasitic extraction of the circuit and the inclusion of circuit pads result in a reduction in performance. Specifically, the layout in Fig. 4.7, without pads, achieves an ENOB of $7.9\,\mathrm{bit}$, representing a reduction of $0.3\,\mathrm{bit}$. The power consumption increases by $1.16\,\mu\mathrm{W}$, reaching $12.25\,\mu\mathrm{W}$, which does not make a significant difference. However, the addition of circuit pads has a substantial impact on the performance of the $\Sigma\Delta$M, reducing the ENOB to $7.68\,\mathrm{bit}$, which is a half-bit difference. At the same time, the power consumption nearly doubles, reaching $20.91\,\mu\mathrm{W}$ due to the biasing of the pads' ESD protection circuit. The next version of the $\Sigma\Delta$M includes additional details concerning post-layout simulations, examining the causes and potential solutions to mitigate it.

The performance of the designed circuit is compared with those presented in Section 2.5, which represent the current state of the art. The shown results are from the pad-less post-layout first $\Sigma\Delta$M version. The relationship between area and power graph in Fig. 4.9 highlights the trade-off between minimal area and low power consumption, comparing the detailed circuits in Section 2.5, the quasi-passive reference $\Sigma\Delta$M and the first ported $\Sigma\Delta$M version. The initial implementation demonstrates promising results, being the smallest $\Sigma\Delta$ converter and positioning it in the favorable region of the graph.

Finally, the FoM_2 and FoM_3 values are calculated, yielding $437.6\,\mathrm{fJ/conv-step}$ and $0.788\,\mathrm{fJ\cdot mm^2/conv-step}$, respectively. These results, depicted in Fig. 4.10, indicate that while the underperformed in terms of FoM_2 from the direct porting process, FoM_3 is reduced by $12\,\%$. Together, the post-layout simulation data and the FoM values provide essential metrics for benchmarking the tape-out version's performance. The following chapter outlines the measurement procedures and discusses challenges encountered during in-silicon testing, comparing this simulation data with the measured results.

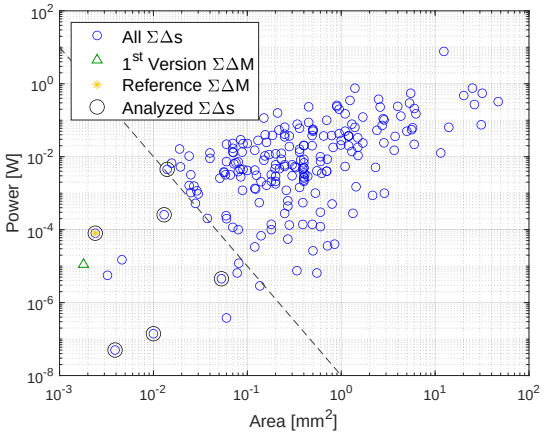
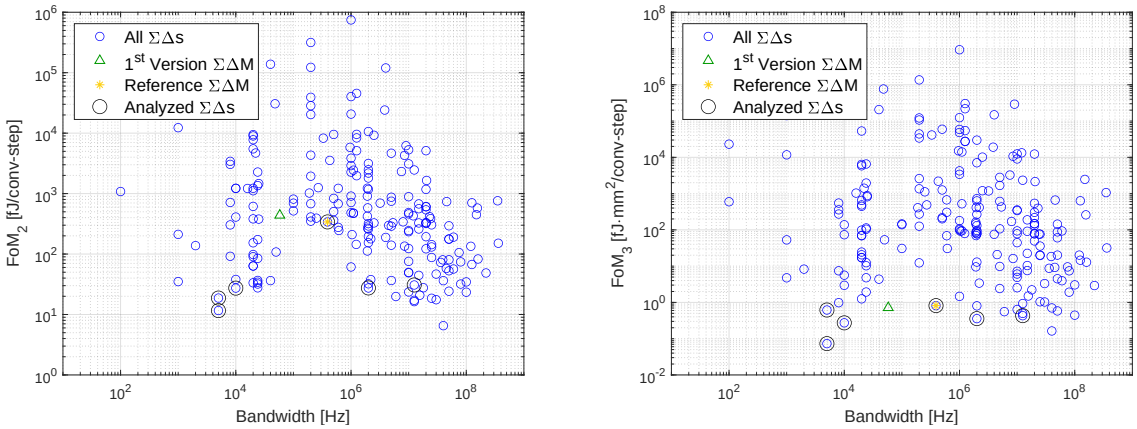


Figure 4.9: Area vs. Power Consumption Analysis considering $\Sigma\Delta$ Converters.



(a) FoM_2 **(b)** FoM_3

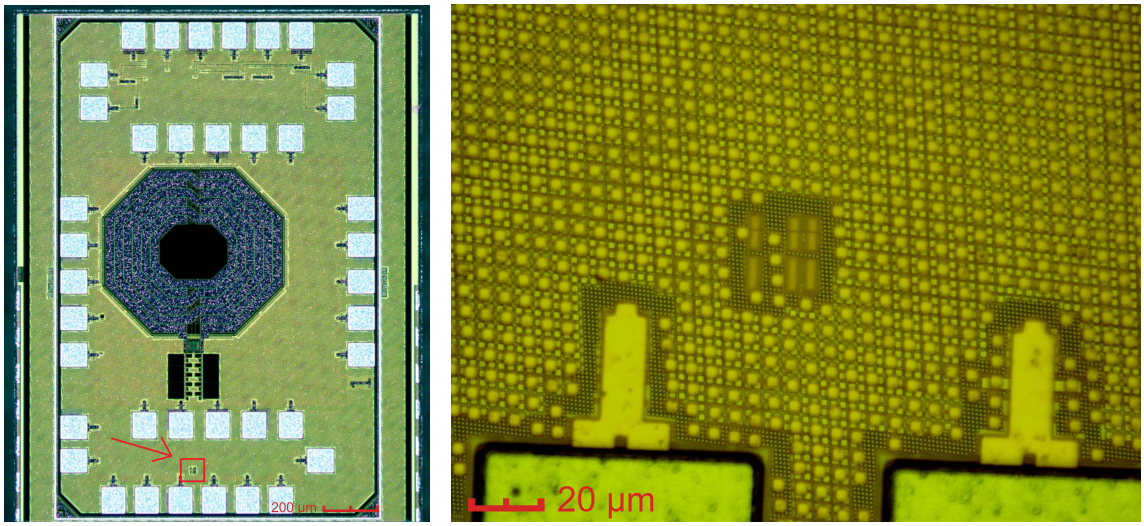
Figure 4.10: FoMs vs. Bandwidth Analysis considering $\Sigma\Delta$ Converters.

Chapter 5

In-Silicon Testing and Validation

The complexity of modern mixed-signal ICs makes validating their correct operation a challenging task. Furthermore, simulating all electrical aspects of the design across all process variations requires significant time and computational resources [57]. In-silicon testing represents a crucial phase in developing ICs. This chapter details the process of verifying the functionality and performance of the fabricated chip. The primary goal is to ensure that the silicon implementation meets the behavior derived from post-layout simulations, thus validating the quasi-passive $\Sigma\Delta$M architecture.

Fig. 5.1 shows two microscopic images of the fabricated IC die, captured at different zoom levels to highlight the various structures and features of the chip. In Fig. 5.1(a), the $\Sigma\Delta$M is highlighted in red, and it can be observed that the chip die is shared among multiple projects within INESC-ID, as mentioned in Section 4.3. Fig. 5.1(b) provides a more detailed close-up, displaying elements such as capacitors and metal interconnects.

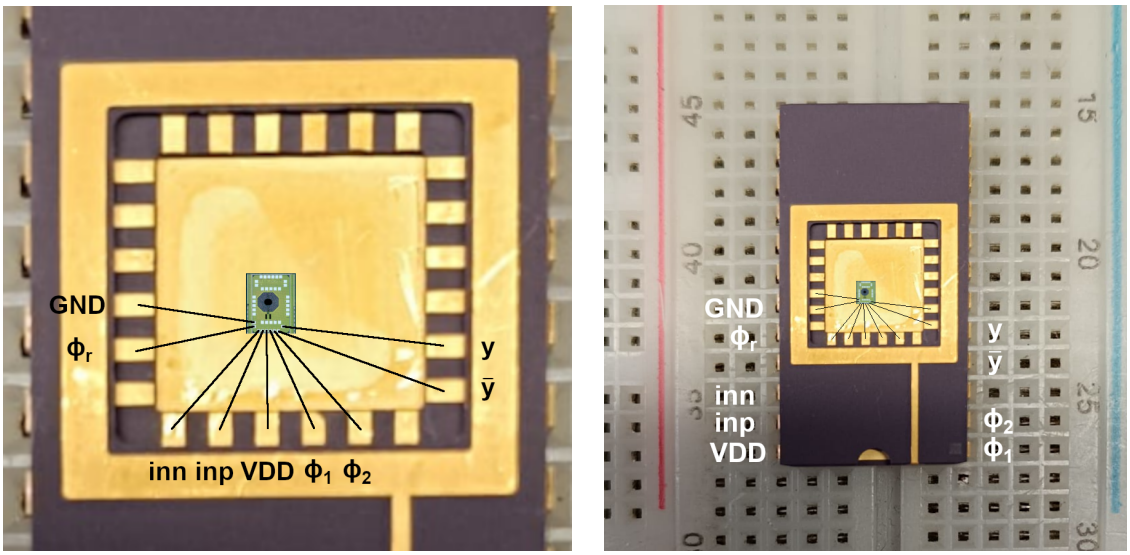


(a) Circuit Die at $35\times$ Zoom

(b) Close-up View at $400\times$ Zoom

Figure 5.1: Microscopic Images of the $\Sigma\Delta$M.

Fig. 5.2 illustrates a diagram of the $\Sigma\Delta$M and its packaging. Fig. 5.2(a) provides a close-up view, while Fig. 5.2(b) displays the 24-pin ceramic chip carrier used for housing and protection of the IC. These figures present the pinout arrangement of the $\Sigma\Delta$M, where each pin serves a distinct function, including power supply (VDD), input signals (inp and inn), output signals (y and $\bar{\mathrm{y}}$), ground (GND), and the non-overlapping control clocks (ϕ_1, ϕ_2, and ϕ_r). As only 9 pins are used per IC, this chip carrier can accommodate two ICs. The slight offset positioning of the IC allows space for a second one to be placed symmetrically and ensures that differential connections, such as the input signal, have similar bonding wire lengths.



(a) Close-Up View

(b) Chip Carrier View

Figure 5.2: $\Sigma\Delta$M Pinout Configuration.

5.1 Wire Bonding

Manual wire bonding is a time-consuming process that requires precision, and several challenges arise during the procedure. In this work, the steps of the bonding process are conducted by the author.

Initially, the IC must be affixed to the chip carrier. This process begins by cleaning the chip carrier with absorbent paper and $99\,\%$ isopropyl alcohol. Subsequently, cyanoacrylate adhesive, commonly known as instant glue, is applied to the chip carrier. The IC is carefully placed on top of the adhesive using tweezers. The adhesive drying process takes around 30 minutes. Once dry, the bond is tested by gently applying pressure to the IC with any fine handling tool. A successful bond will exhibit high resistance to movement, while insufficient bonding will cause the IC to shift, requiring the process to be repeated.

The wire bonding process is conducted using a manual wire bonding machine, model 4123 Universal Wedge Bonder from Kulicke and Soffa® Industries, depicted in Fig. 5.3. The machine operates according to the procedures established in the INESC-MN laboratory, utilizing $25\,\mu\mathrm{m}$ wire. The machine parameter configuration is provided in Fig. 5.3(b).

(a) Top View **(b)** Parameter Configuration

Figure 5.3: Wire Bonding Machine.

Ensuring that no short circuits occur between the pads is an essential part of the procedure, as such issues can lead to chip malfunction or failure. The bondings are inspected under a microscope to verify that each one is properly connected. Fig. 5.4 illustrates an example where a short circuit is detected in the bonding, marked in red, requiring its disposal. In contrast, a correctly functioning connection is marked in green.

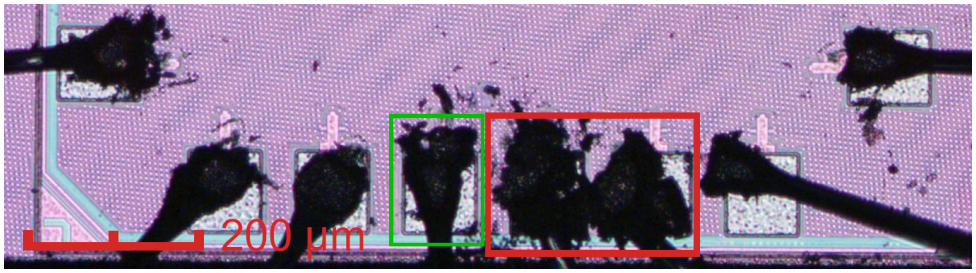
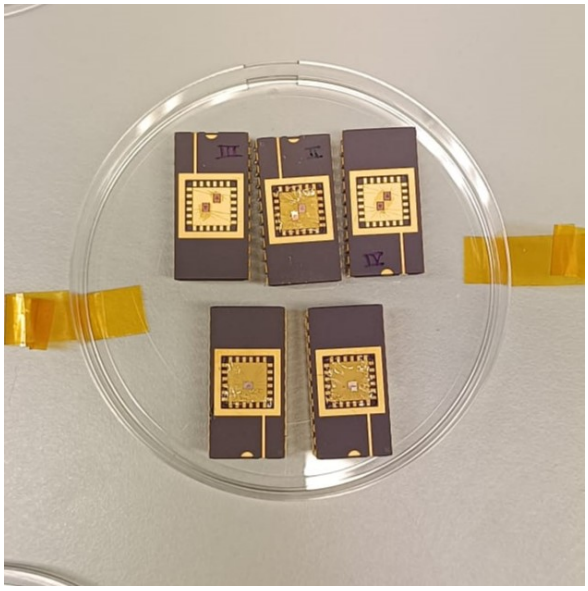


Figure 5.4: Example of a Bonding with Short Circuit.

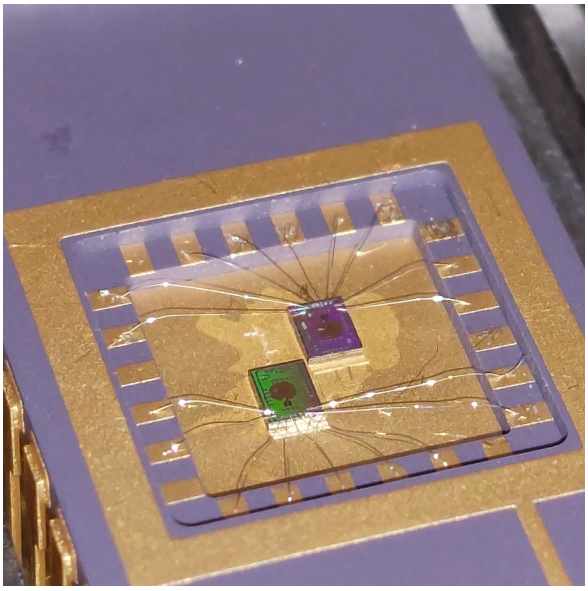
The next IC version should prioritize pad layouts that facilitate the bonding process by increasing the distance between pads or optimizing their arrangement based on the intended chip carrier. This approach aims to simplify the bonding process and improve wire yield, thereby reducing the need to discard short-circuited chips. Nonetheless, eight wire-bonded chips are prepared for testing, as seen in Fig. 5.5(a). Fig. 5.5(b) presents an example chip carrier containing two ICs. This approach reduces the number of chip carriers required and enhances testing efficiency. A close-up view of the wired pads is also provided in Fig. 5.5(c).

5.2 Test Bench Setup

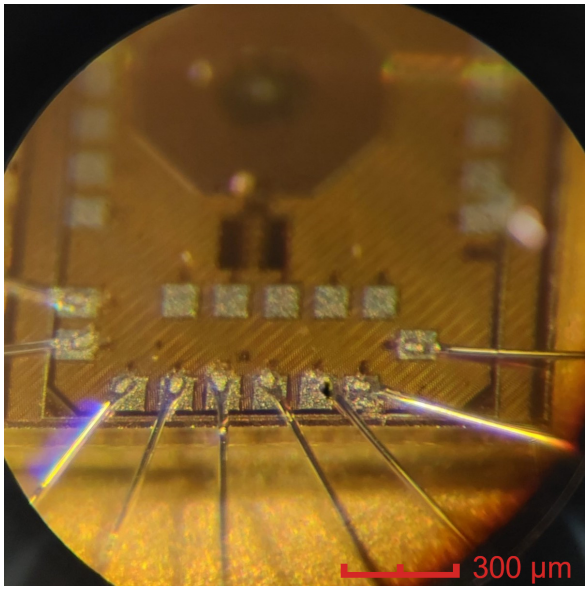
Several conditions must be arranged to test the encapsulated and wired $\Sigma\Delta$Ms. These include a supply voltage of $1.2\,\mathrm{V}$, three non-overlapping clock signals ranging from ground to $1.2\,\mathrm{V}$ at a sampling frequency of $15\,\mathrm{MHz}$, and an input signal with an amplitude of $200\,\mathrm{mV}$ at a frequency of $20141.6\,\mathrm{Hz}$.



(a) All Encapsulated Chips



(b) Top View of Wire Bonding

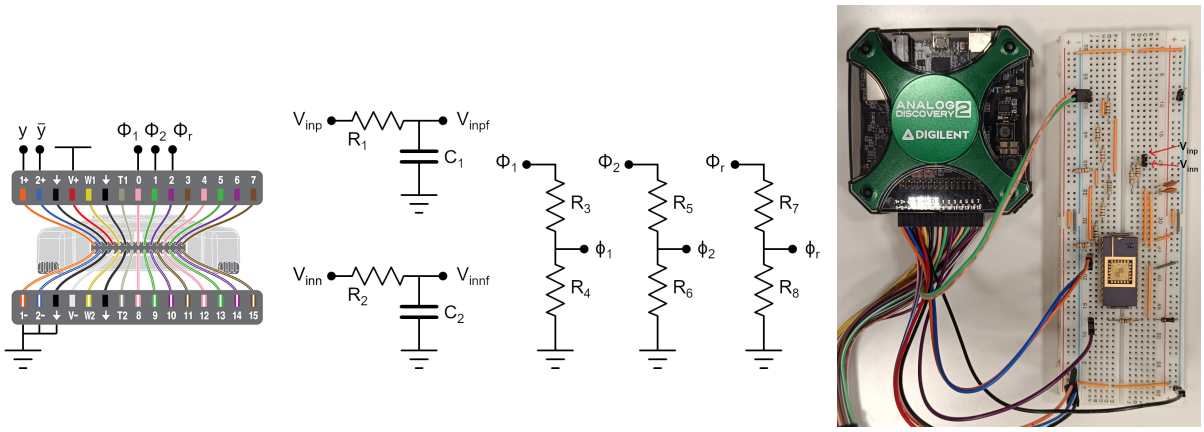


(c) Close-Up of Wire Bonds

Figure 5.5: Encapsulated and Wire Bonded $\Sigma\Delta$Ms.

To enable testing without the need to wait for a custom printed circuit board (PCB) to be manufactured, and given that the tape-out of the circuit is intended to validate simulations and the proposed architecture, the chips are tested using a Digilent® Analog Discovery 2. The Digilent® Analog Discovery 2 is an USB oscilloscope, logic analyzer, and multi-function instrument that enables the measurement, visualization, generation, recording, and control of mixed-signal circuits. The device is a compact and cost-effective oscilloscope, capable of being used as a portable instrument, and is operated through the free Digilent WaveForms software [58].

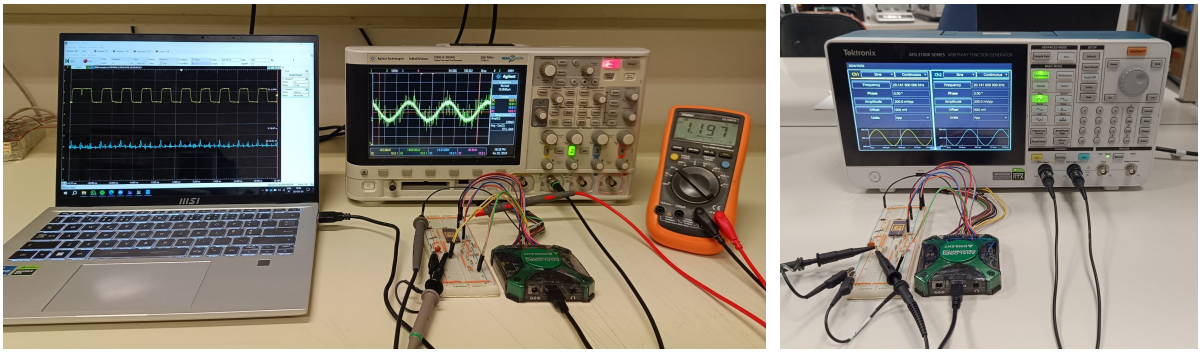
The test setup consists of using the two-channel USB oscilloscope for logging the output, three channels of a 16-channel pattern generator to generate non-overlapping clocks and one of the two programmable power supplies [59, 60]. A challenge arises from the pattern generators, which operate between ground and $3.3\,\mathrm{V}$. While a voltage divider could address this issue, selecting appropriate resistances presents difficulties. High resistances in parallel with the output cause clock signal attenuation, while low resistances cause problems with driving capability. The optimal configuration results in a voltage divider using resistances of $1.2\,\mathrm{k\Omega}$ and $2.1\,\mathrm{k\Omega}$. Furthermore, two RC LPFs are designed for the input signals, utilizing a capacitance of $120\,\mathrm{nF}$ and a resistance of $27\,\Omega$, resulting in a cutoff frequency of $49.1\,\mathrm{kHz}$. The setup configuration is shown in Fig. 5.6.



(a) Circuit Diagram **(b)** Breadboard Implementation

Figure 5.6: Test Bench Representation.

Although the Analog Discovery 2 is capable of generating input signals and is used during initial prototyping, the AFG31000 Series Arbitrary Function Generator by Tektronix® is employed for chip testing to achieve less noisy results. This generator offers a resolution of $14\,\mathrm{bit}$ and up to three times greater accuracy than the Analog Discovery 2 [61]. Examples of the complete test bench setup are shown in Fig. 5.7.



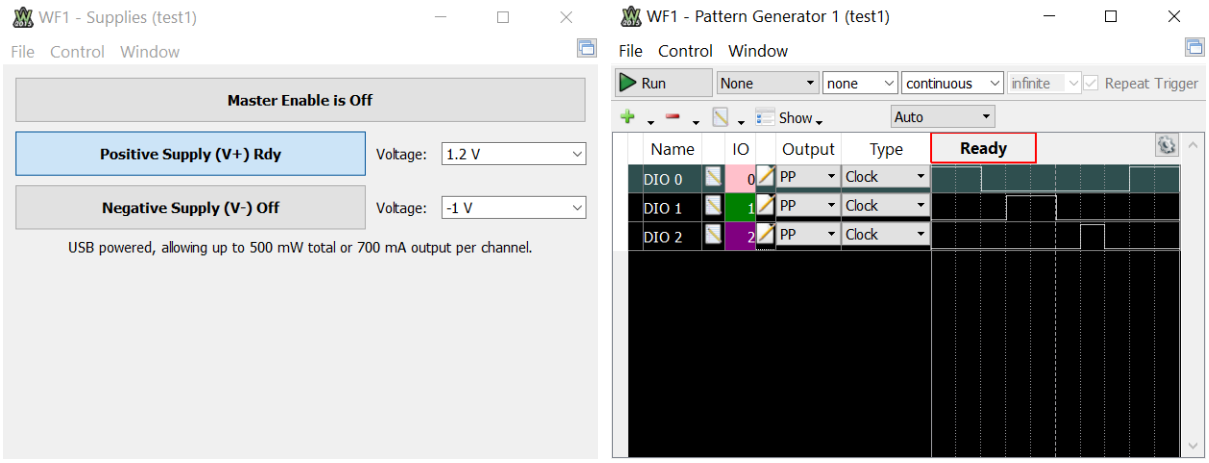
(a) Using Analog Discovery 2 only **(b)** Using Tektronix AFG31000 Series

Figure 5.7: Complete Test Bench Configurations for Chip Testing.

Finally, a temporary resistor is placed in series with the power supply to measure power consumption. The resistor is only utilized during this measurement process. The average or DC voltage across this resistor is measured using a laboratory oscilloscope. The power consumption can then be calculated using V^2/R. The value of the resistor must be selected appropriately. As mentioned in Section 4.4, the circuit is expected to draw $17\,\mu\mathrm{A}$. The chosen resistor should generate a voltage across its terminals in the range of a few mV with this current, sufficient for the oscilloscope to detect while ensuring the supply voltage to the $\Sigma\Delta$M does not drop significantly below $1.2\,\mathrm{V}$. For this reason, a resistor of $180\,\Omega$ is used.

5.3 Testing Procedure

Upon setting up the presented test bench, the $\Sigma\Delta$M is ready for testing. At this stage, a simple configuration is required in the Digilent WaveForms software. The supply voltage and non-overlapping clocks are configured using the Supplies and Patterns forms, respectively, as shown in Fig. 5.8. Both configurations should follow the one provided.



(a) Supply Voltage **(b)** Non-Overlapping Clocks

Figure 5.8: WaveForms Software Interface for Configuration.

Proper setup in the WaveForms software should prevent issues in the circuit under test. However, verifying the Analog Discovery 2 outputs before connecting them to the $\Sigma\Delta$M is recommended. This verification can be done using a multimeter for the supply voltage and any standard laboratory oscilloscope for the non-overlapping clocks. It is important to ensure that the supply voltage is always turned on before the clocks and that the clocks are turned off before the supply voltage is turned off to prevent damage to the chip.

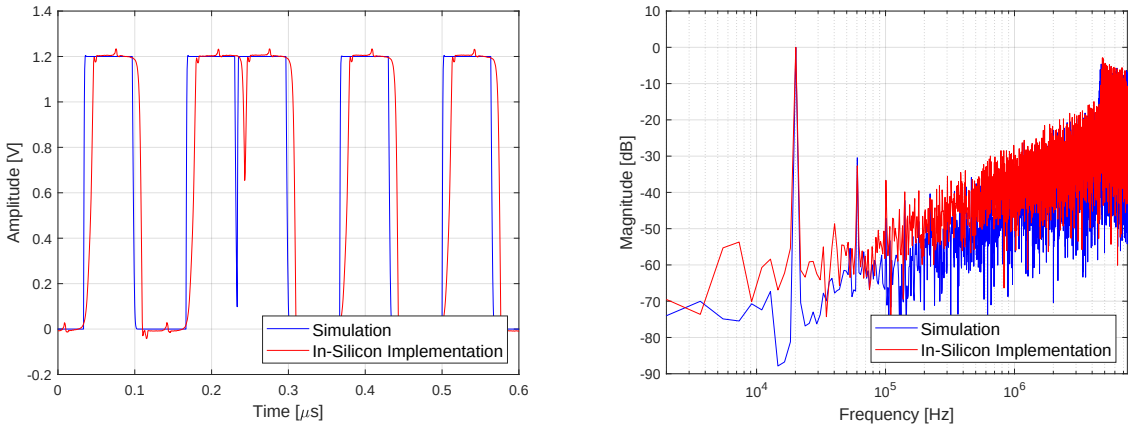
Once the function generator is configured as shown in Fig. 5.7(b), and the supply and clocks are activated, the input waveforms can be turned on by pressing the yellow and blue buttons on each output channel, also visible in Fig. 5.7(b). The output waveforms should begin to resemble the simulation results, and these signals

can be acquired using the Scope or Logger functions of the WaveForms software. Finally, the resolution of the acquired output can be calculated using the Python3 script, as described in Chapter 4.

The power consumption measurements should be conducted without an output load connected to minimize the introduction of additional variables into the circuit testing, as load values inherently have tolerances.

5.4 Measured Results

The following section presents a comparison between the simulated and measured results. Fig. 5.9(a) shows the waveform comparison for an example case. The signals exhibit similar characteristics, with the main difference being the output load, which appears to be higher for the in-silicon $\Sigma\Delta$M, resulting in increased rise and fall times. Additionally, the silicon implementation demonstrates some unexpected behavior, including voltage spikes occurring in the middle of each bit value. This phenomenon can be attributed to charge leakage caused by parasitic capacitances. Fig. 5.9(b) illustrates the comparison between the simulated DFT and the measured data average DFT. The measured DFT reveals second-order effects, primarily caused by layout asymmetries and different sizes of bonding wires, affecting the system's differential balance [56].



(a) Output Signals Example

(b) DFT Comparison

Figure 5.9: Comparison Between Simulation and In-Silicon Measurements.

The results from simulations and measurements are summarized in Tab. 5.1. The post-layout simulation indicates an ENOB of $7.68\,\mathrm{bit}$, whereas the measured ENOB values range from $4.56\,\mathrm{bit}$ to $7.31\,\mathrm{bit}$, with an average of $5.73\,\mathrm{bit}$. These differences illustrate the impact of real-world factors, such as bonding wires, voltage supply inaccuracies, and clock imperfections, which are not accounted for in simulations. Including these factors in simulations would also result in lower simulated resolution. Additionally, bonding imperfections may persist despite microscopic verification, indicating that circuits with significantly reduced resolution likely exhibit connection issues.

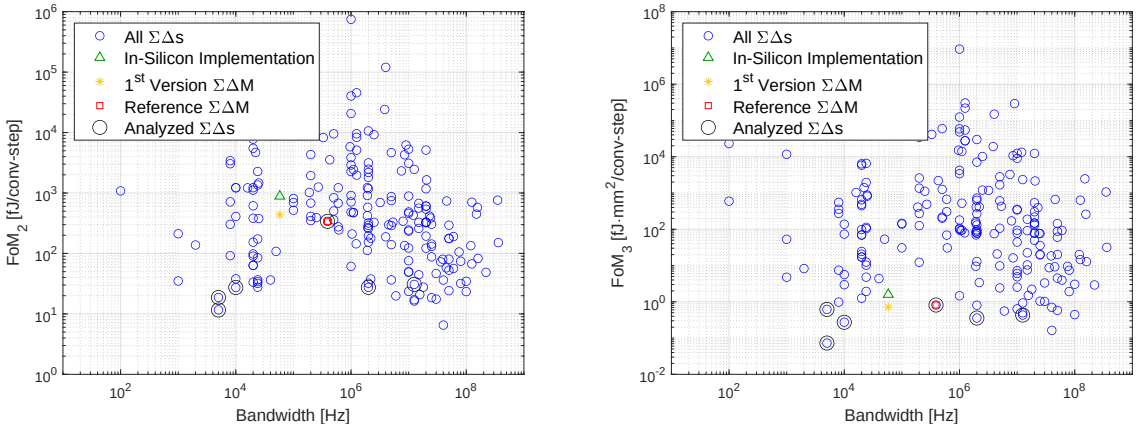
The simulated power consumption without output load is $10.09\,\mu\mathrm{W}$, while the measured power consumption is around half, at $5.46\,\mu\mathrm{W}$. This discrepancy is presumably due to uncertainty in the power consumption calculation method. However, since the values are within the same order of magnitude, a more accurate calculation method would lead to better alignment between the results.

Table 5.1: Performance Metrics Comparison Between Simulation and In-Silicon Measurements.

Tested Metric	**Simulation**	**In-silicon Measurements**		
		Min.	**Avg.**	**Max.**
ENOB [bit]	7.68	4.56	5.73	7.31
Power Consumption [μW]	10.09	-	5.46	-

The uncertainties and differences between the simulations and the taped-out circuit are within acceptable range to validate the functional aspect of the $\Sigma\Delta$M architecture. However, these variations indicate the need to revise the testing procedure for the next tape-out. Additionally, utilizing a custom PCB is expected to produce more accurate results and better align with the simulation outcomes.

The FoM_2 and FoM_3 values are calculated using the average measures, as done previously in Section 4.4, resulting in $883.9\,\mathrm{fJ/conv-step}$ and $1.591\,\mathrm{fJ\cdot mm^2/conv-step}$, respectively. These results, shown in Fig. 5.10, indicate a two times increase in each FoM, attributed to a two-bit difference in ENOB and a reduction in power consumption by half.



(a) FoM_2 **(b)** FoM_3

Figure 5.10: FoMs vs. Bandwidth Analysis considering $\Sigma\Delta$ Converters.

Finally, with these measured results validating the performance of the quasi-passive $\Sigma\Delta$M architecture, the next chapter focuses on optimizing the simulation workflow prior to enhancements in the $\Sigma\Delta$M implementation.

Chapter 6

Simulation Optimization Strategies

Efficient use of computational resources on the INESC-ID remote machine is critical. Optimizing simulations and the workflow earlier allows for greater efficiency when addressing circuit-level improvements on the $\Sigma\Delta$M. The circuit simulations are run on a Linux system featuring an Intel® Core™ i7-4771 CPU with 8 cores, operating at $3.50\,\mathrm{GHz}$, $24\,\mathrm{GB}$ of system memory, and $1.8\,\mathrm{TB}$ of disk space shared among 20 users. Given the system's specifications and shared usage, resource optimization is essential. This chapter presents, without extensive detail, the strategies employed to improve performance and automate processes, along with the associated enhancements in speed and resource efficiency. The syntax of specific functions and their usage is simplified throughout this chapter, as it is intended only for descriptive purposes.

6.1 Original Workflow

The initial workflow for operating the $\Sigma\Delta$M involves designing the circuit in Cadence® Virtuoso® Analog Design Environment (ADE) and simulating it using Spectre® Accelerated Parallel Simulator (APS), with the desired waveforms saved through Verilog-A blocks [54]. These blocks sample the waveforms and store the data in a $.\mathrm{csv}$ file. A Python3 script is subsequently used to calculate the DFT and extract the dynamic performance metrics described in Section 2.2.2. This workflow is performed for transient simulations, which, despite being computationally intensive, are preferred for their accuracy in reflecting circuit functionality.

Two specific challenges are identified in this process. The first challenge involves having different tools, namely using Cadence® Virtuoso and measuring resolution with Python3. This approach makes circuit optimization a highly manual task, which ideally should be automated and limits the ability to conduct MC simulations. Additionally, the Verilog-A blocks, which open and write large data files at different simulation stages, introduce further inefficiencies, potentially causing significant simulation delays depending on the file sizes.

6.2 Simulation Refinement

The main challenge in utilizing the Cadence® Virtuoso calculator for evaluating circuit resolution arises when calculating the linearity of the front-end, which is analyzed in the charge domain. This expression is particularly complex, as it determines the differential charge variation between sampling iterations. To clarify the problem and its solution, the circuit under analysis is illustrated in Fig. 6.1.

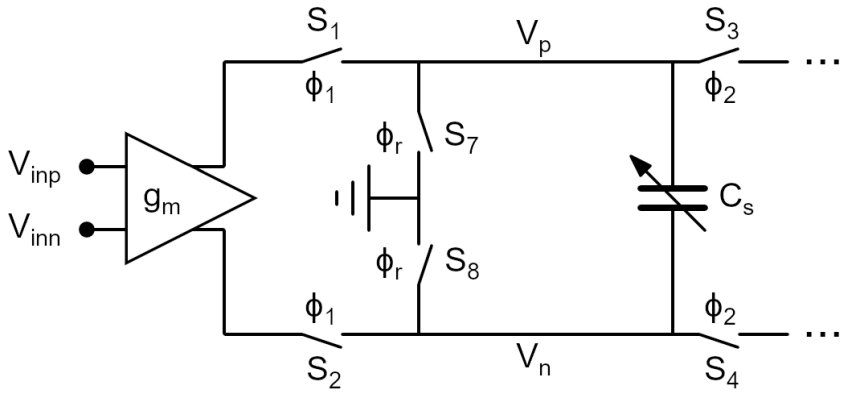


Figure 6.1: ΣΔM Front-End Schematic.

Using the Verilog-A data saver block can be avoided by applying the iinteg function to selected waveforms in Cadence® Virtuoso. The iinteg integral function computes the indefinite integral of the buffer expression concerning the X-axis variable, which corresponds to the time during transient simulations. Thus, the charge is obtained by applying the iinteg function to the output current of the switches S_1 and S_2, as shown in (6.1). Subtracting these charges yields the differential charge, as seen in (6.2).

$$Q_{S_{1,2}} = \mathrm{iinteg}(I_{S_{1,2}}) \tag{6.1}$$

$$Q_{diff} = Q_{S_1} - Q_{S_2} \tag{6.2}$$

However, Q_{diff} does not represent the variation between sampling iterations Q_Δ. To calculate Q_Δ, Q_{diff} is shifted by one clock cycle using the rshift function. Subtracting the original Q_{diff} and the shifted version provides the desired differential charge variation between sampling iterations, as shown in (6.3).

$$Q_\Delta = Q_{diff} - \mathrm{rshift}(Q_{diff}\ 1/f_s) \tag{6.3}$$

A comparison of the resulting waveforms from both procedures is done to verify that similar results are obtained, as illustrated in Fig. 6.2. The results are consistent, with a difference in the maximum charge of $0.0054\,\mathrm{fC}$.

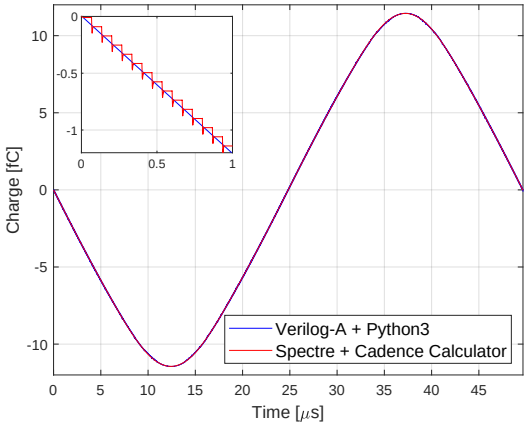
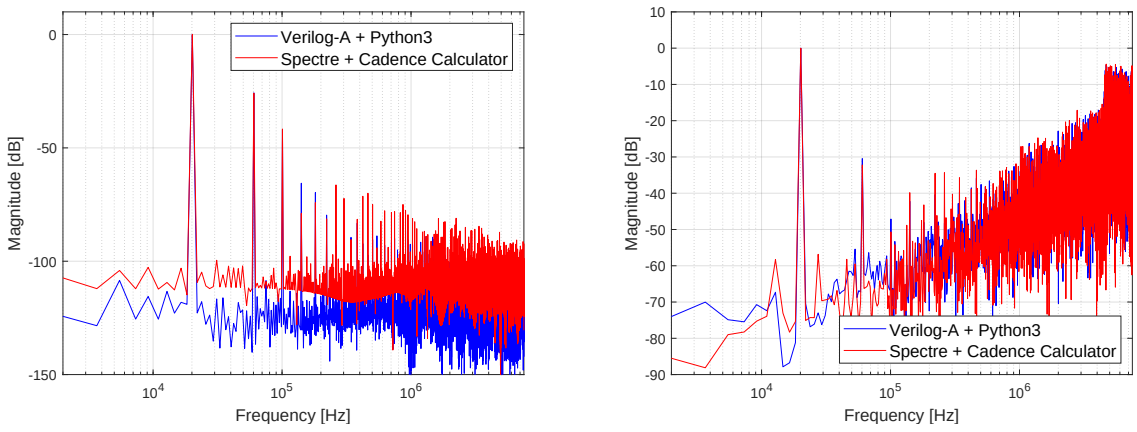


Figure 6.2: Comparison of the Charge Waveform from both Procedures.

At this stage, the necessary waveforms for resolution calculation, Q_Δ and the $\Sigma\Delta$M output y, are available. The next step involves determining a method to calculate performance directly using Cadence® Virtuoso calculator functions. This procedure is achieved by utilizing the DFT function within Cadence® Virtuoso, from which the dynamic performance metrics can be calculated through the $\mathrm{spectrumMeas}$ function with the appropriate arguments. The resulting DFTs are depicted in Fig. 6.3.



(a) Front-End Charge DFT

(b) $\Sigma\Delta$M Output DFT

Figure 6.3: Comparison of the DFTs across Different Procedures.

Although visual differences are evident in terms of DFT, the magnitudes of the harmonics remain similar. The computed dynamic performance metrics support this observation, with the ENOB values presenting a negligible maximum difference of $0.018\,\mathrm{bit}$, as indicated in Tab. 6.1. This result validates the procedure that avoids the use of Python3, which facilitates the simulation process. It also significantly reduces the demand for simulation resources, as later elaborated in Section 6.4.

Table 6.1: Performance Comparison across Different Procedures.

Tested Block	ENOB using Python3 [bit]	ENOB using Cadence® [bit]	ENOB Difference [bit]
Front-End	3.965	3.983	0.018
Complete ΣΔM	8.178	8.195	0.017

6.3 Advanced Simulation Techniques

Spectre® APS is an important tool for evaluating circuit designs, particularly for analog and mixed-signal designers, verification engineers, and CAD professionals. This section provides insights into optimizing the performance of Spectre® APS for analog and mixed-signal applications through essential configuration options.

Two primary options are available to balance accuracy and performance during simulations: $\mathrm{errpreset}$ and $++\mathrm{aps}$. The $\mathrm{errpreset}$ option, which can be set to $\mathrm{conservative}$, $\mathrm{moderate}$, or $\mathrm{liberal}$, determines the solver tolerances. The $\mathrm{conservative}$ setting produces the highest accuracy, whereas the $\mathrm{liberal}$ setting maximizes performance. The $++\mathrm{aps}$ option enhances performance for each $\mathrm{errpreset}$ configuration, typically achieving a 1.5 to 2 times performance improvement over simulations using $+\mathrm{aps}$, while maintaining similar accuracy [62]. These options are configurable in the High-Performance Simulation Options form within Virtuoso® ADE.

The $+\mathrm{mt}$ option enables multithreading, improving Spectre® APS performance compared to single-threaded simulations. The number of threads can also be specified in the High-Performance Simulation Options form.

At INESC-ID Virtuoso® ADE, the $++\mathrm{aps}$ option is enabled by default, and multithreading is generally discouraged due to frequent crashes. Furthermore, under the output Save Options form in Virtuoso® ADE, all voltage nodes are set to be saved by default. This practice leads to inefficiencies resulting from excessive data storage and memory consumption. As demonstrated in the results presented in the following section, it is critical to configure the output Save Options to retain only the selected signals.

6.4 Performance Comparison

Speed-up measurements are essential for evaluating the efficiency and effectiveness of different systems or configurations. By measuring performance metrics, such as resource utilization and execution time, it becomes possible to identify bottlenecks, inefficiencies, and areas for improvement.

A distinction between CPU and elapsed time is first required for proper comparison analysis. CPU time refers to the actual processing time utilized by the CPU to execute the simulation, which is important for assessing the computational intensity. Elapsed time, on the other hand, is the total duration required to complete the simulation, including CPU time and any additional delays due to resource waits, such as memory access, network latency, or lock waits. Elapsed time provides a more comprehensive measure of the overall time a simulation takes from start to finish. High CPU time may indicate computational inefficiency, while high elapsed time with low CPU time may suggest delays from resource contention.

Three different sets of simulations are conducted to evaluate the impact of different optimization techniques. The base simulation measures the performance without any optimizations. Simulation 1 involves simulating without Verilog-A blocks, saving only selected signals, and using the $\mathrm{conservative}$ option. Simulation 2 is identical to simulation 1, except for using the $\mathrm{liberal}$ option. Performance under the different configurations is evaluated without multithreading, with results averaged over 10 samples per test and presented in Tab. 6.2. No other processes are executed during these experiments to ensure accurate benchmarking.

Table 6.2: Time Performance Comparison across Different Procedures.

Tested Block	**Base Times** [s]		**Simulation 1 Times** [s]		**Simulation 2 Times** [s]	
	CPU	**Elapsed**	**CPU**	**Elapsed**	**CPU**	**Elapsed**
Front-End	392	746	206	209	102	103
Complete ΣΔM	1613	2059	1527	1532	570	572

The results in Tab. 6.2 allow some conclusions to be drawn. As anticipated, the base implementation demonstrates poor memory usage efficiency, as indicated by the difference of 1.3 to 2 times between CPU and elapsed time. In simulations 1 and 2, the CPU and elapsed times are nearly identical, resulting in close to $100\,\%$ CPU utilization throughout the simulations, which is optimal. When comparing elapsed times, simulation 1 achieves a speed-up of 3.6 and simulation 2 acquires 7.2, for the front-end simulations. For the complete ΣΔM tests, simulation 1 reaches a speed-up of 1.3, and simulation 2 attains 3.6. Notably, these results do not account for the additional time spent managing files and running Python3 scripts, estimated to add 5 minutes on average to the total base simulation time. Overall, the approach significantly enhances the simulation process.

The difference in elapsed times between simulations 1 and 2 suggests that the $\mathrm{liberal}$ option should be preferred. However, as discussed in Section 6.3, this option produces a less accurate simulation, resulting in a half-bit difference in ENOB and a $0.2\,\mathrm{fC}$ difference in maximum charge variation in the front-end simulation. In this context, the difference is considered significant due to its implications for the design of the feedback capacitors. In the complete ΣΔM, however, the difference of $0.2\,\mathrm{bit}$ in ENOB is considered negligible.

6.5 Remote Automation

Secure Shell (SSH) is the protocol used to securely access INESC-ID remote Linux servers and utilize development tools, like Cadence® Virtuoso® ADE. One notable disadvantage is that any interruption in the internet connection maintaining the SSH session results in the termination of active user processes. Although Virtuoso® ADE can save data under these circumstances, simulations in progress generally require restarting. This issue is particularly relevant for the time-consuming simulations discussed in Section 6.4, especially when running MC simulations.

The application Screen can be utilized to address these challenges. Screen is a Linux terminal multiplexer that allows the user to start a session and open multiple windows within that session. Processes running in Screen continue even if the window is not visible or the user is disconnected. With this solution, managing simulations within a Screen session becomes feasible.

Cadence® Virtuoso primarily uses SKILL as its scripting and automation language. SKILL is a programming language that facilitates task automation, workflow customization, and interaction with design data. In the context of this work, SKILL scripts are used to run preconfigured ADEXL simulations from Virtuoso® ADE, reducing the complexity of learning a new syntax and maximizing simulation outcomes. The script, provided in Chapter A, can be used for any pair of cell and cell view within the same library. This script executes simulations sequentially, ensuring that only one core is used to minimize conflicts between users, improve resource efficiency, and prevent crashes. Instructions for executing the script are provided in Listing 6.1.

Listing 6.1: Command for Executing SKILL Scripts in Virtuoso.

```
$ virtuoso -nograph -restore script.il
```

The conditions are now suitable for enhancements in the first $\Sigma\Delta$M version circuit, aiming to develop a high-performance converter that meets the objectives outlined in Section 1.2. The next chapter details the process that results in an improved final $\Sigma\Delta$M version.

Chapter 7

Development of the Optimized $\Sigma\Delta$ Modulator

In this chapter, the development and optimization process of the quasi-passive $\Sigma\Delta$M, implemented in $65\,\mathrm{nm}$ technology, is discussed. The process begins with enhancements at the building block level, followed by the design and addition of clock generation, and concludes with layout optimizations. The final chip design is then presented, along with simulations and validation of the developed solution.

7.1 Design Optimizations

Optimization at the building block level is essential in enhancing the performance and efficiency of the $\Sigma\Delta$M. This phase emphasizes factors such as power consumption, area, and robustness of each block. The strategy involves minimizing the complexity of individual components while improving their overall functionality. The comparator is not subject to design changes, as the design presented in Section 4.1.4 is already effective.

7.1.1 Transconductance Cell

The g_m cell is a crucial component in the $\Sigma\Delta$M. One limitation of the initial design is the presence of R_S, which represents the series resistance equivalent of the series transistors, as discussed previously in Section 3.2.1. However, the noise performance and dynamic range can be optimized by removing the transistors responsible for switching the cell on and off.

A modified design is proposed where the gate voltage of the CMFB PMOS transistors is controlled by a clock signal. This modification maintains the ability to switch the g_m cell on and off and is anticipated to enhance the dynamic range and noise performance while utilizing the same number of transistors and omitting the switch transistors from the signal path. The implementation is depicted in Fig. 7.1.

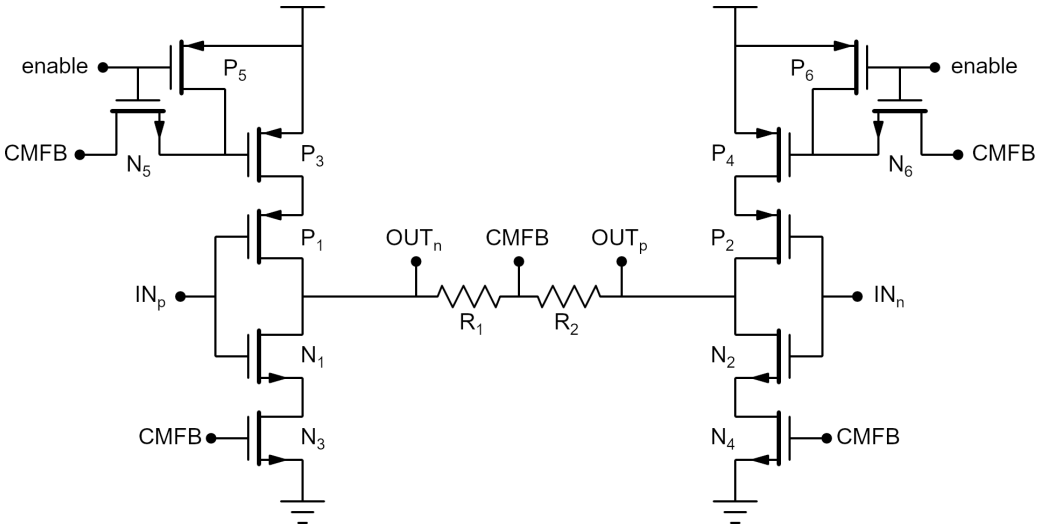


Figure 7.1: Final g_m Cell Circuit Schematic.

A primary concern with this design is the risk of a low-impedance path. This issue is mitigated by implementing transistors N_5, N_6, P_5, and P_6 with high V_{th} to ensure sequential switching. These transistors are minimized in size to conserve area, as no signal current passes through them, eliminating the need for low R_{on} or high linearity. The remaining transistor dimensions are optimized using Virtuoso® ADE tools. The remaining NMOS and PMOS transistors are implemented as low V_{th} and are sized equally for layout simplicity and improved matching. The aspect ratios between NMOS and PMOS follow a $1{:}4$ proportion to compensate for electron mobility and to ensure a balanced g_m cell, as later demonstrated. Additionally, the sensing resistors are downsized to $40\,\mathrm{k\Omega}$ to reduce area usage, as discussed in Section 4.3. Tab. 7.1 summarizes the dimensions of the updated circuit elements.

Table 7.1: Final g_m Cell Transistors Dimensions.

Circuit Element	$P_{1,2,3,4}$	$N_{1,2,3,4}$	$P_{5,6}$ / $N_{5,6}$	$R_{1,2}$
Width [µm]	0.6	0.15	0.2	0.4
Length [µm]	0.9	0.9	0.06	21.05

The g_m and R_{on} of the transistors are analyzed to assess whether the g_m cell is balanced and to validate the derived expressions in Section 3.2.1. These values are provided in Tab. 7.2. The variation in these parameters is less than $20\,\%$, indicating that the cell is sufficiently balanced. In this implementation, the circuit expressions can be simplified as shown in (7.1) and (7.2), resulting in an expected G_m of $34.3\,\mathrm{\mu S}$. However, as discussed in Section 3.2.1, these expressions do not account for the body effect, which may result in deviations.

Table 7.2: g_m and R_{on} Values for the Transistors in the g_m Cell.

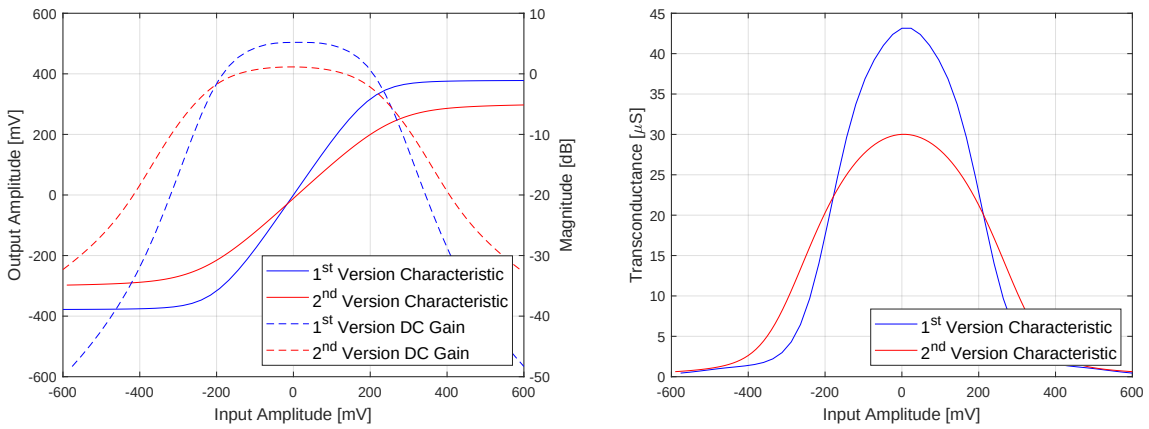
Transistors	$\boldsymbol{g_m}$ [µS]
$P_{1,2}$	17.1
$N_{1,2}$	14.0

Transistors	$\boldsymbol{R_{on}}$ [kΩ]
P_3 / P_4	53.5
N_3 / N_4	50.7

$$g'_m = \frac{g_m}{1+g_m \cdot R_{on}} \tag{7.1}$$

$$G_m = 2 \cdot (g'_{m_n} + g'_{m_p}) \tag{7.2}$$

Finally, Fig. 7.2 presents the DC characteristics of the two versions of the g_m cell. As described in Section 4.1.1, the objective is to achieve a linear gain region over a broad range of input voltages. This implementation exhibits a linear gain across an input voltage range of $395\,\mathrm{mV}$, representing an improvement of $20\,\%$ compared to the first version, which is highly favorable. The dynamic range is reduced to $595\,\mathrm{mV}$, but this reduction does not decrease performance, as demonstrated later. The removal of transistors and the optimization process result in a $40\,\%$ noise reduction. Furthermore, the G_m behavior shows improved linearity, with a maximum value measured at $30\,\mu\mathrm{S}$, resulting in an absolute error of only $12.5\,\%$ when compared to the analytically calculated result. The performance metrics of the final version of the g_m cell are summarized in Tab. 7.3.



(a) DC Transfer Function and Gain

(b) Transconductance vs. Input Voltage

Figure 7.2: g_m Cell DC Characteristics Implementation Comparison.

Table 7.3: Final g_m Cell Performance Metrics.

A_0 [dB]	**Bandwidth** [MHz]	**Dynamic Range** [mV]	G_m [μS]	V_n [nV]
1.14	8.1	595	30	83.7

7.1.2 Bootstrapped Switch

The bootstrapped switch schematic remains unchanged, as shown in Fig. 7.3, but analyzing its behavior presents challenges. As discussed in Section 3.2.2, to ensure that C_b charges to the supply voltage during the hold mode, the series combination of P_1, C_b, and N_1 must exhibit a time constant less than half of the clock period. The on-resistance of N_3 should also be minimized to improve performance.

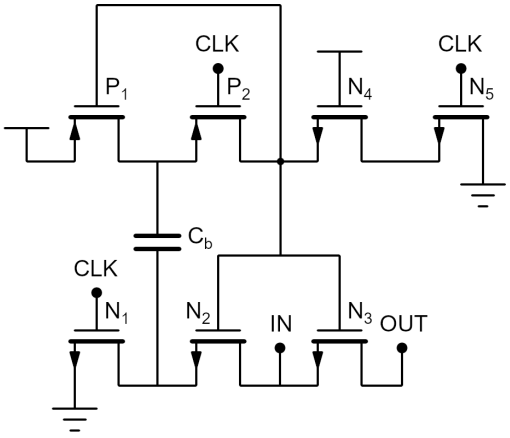


Figure 7.3: Bootstrapped Switch Circuit Schematic.

Charge leakage occurs through the gate of switch N_3, resulting in an overshoot at the output voltage when the switch transitions to hold mode. This overshoot is due to charge transfer from C_b to the output load, degrading the switch's ability to maintain the correct output voltage. Additionally, the relationship between the switch load capacitance and C_b has an impact on this behavior. While this relationship is difficult to characterize analytically [63], it should be considered when sizing C_b, as it impacts the switch's performance.

Most transistors in the bootstrapped switch are maintained with a width of $200\,\mathrm{nm}$ and a length of $60\,\mathrm{nm}$. However, the N_3 switch is set to the minimum possible size, with a width of $120\,\mathrm{nm}$ and a length of $60\,\mathrm{nm}$, to reduce on-resistance. The capacitor C_b is sized at $6\,\mathrm{fF}$ following performance optimization, which corresponds to a MOM capacitor with dimensions of $3.7\,\mu\mathrm{m}$ by $3.2\,\mu\mathrm{m}$. This sizing minimizes charge leakage through the gate of N_3 and represents a reduction in C_b by a factor of three compared to the initial design. The time constant formed by the series combination of P_1, C_b, and N_1 is $40.6\,\mathrm{ps}$ and given a T_s of $66.7\,\mathrm{ns}$, this time constant does not present any issues.

7.1.3 MOSCAPs

In addition to the expected resizing due to optimization using Virtuoso® ADE tools, a significant modification is made to the MOSCAP design to minimize area. As discussed in Section 4.1.3, reducing the aspect ratio of the transistor functioning as a MOSCAP increases the capacitance variation between different operating zones. For example, C_s, designed with a width W of $160\,\mathrm{nm}$ and a length L of $10\,\mu\mathrm{m}$, is implemented using 12 MOSCAPs in parallel ($m=12$), resulting in a total capacitance of $280\,\mathrm{fF}$. This design resultes in a layout of $10\,\mu\mathrm{m}$ by $5.8\,\mu\mathrm{m}$, doubled for its complementary implementation. However, the area compromise is substantial, as this structure has $m-1$ empty gaps between each diffusion deposit. A MOSCAP measuring $10\,\mu\mathrm{m}$ by $5.8\,\mu\mathrm{m}$ achieves a total capacitance of $700\,\mathrm{fF}$, yielding a capacitance increase of 2.5 times for the same area. The higher variation in capacitance zones does not correspond to the area and maximum capacitance gains between implementations. Consequently, to achieve the most compact implementation, m is set to 1 for each MOSCAP in the final design. Although, as a result, a higher $\frac{W}{L}$ ratio is utilized, it remains lower than 1.

The resizing results in C_s having a width of $5\,\mu\mathrm{m}$ and a length of $6\,\mu\mathrm{m}$, resulting in a $380\,\mathrm{fF}$ MOSCAP. For C_{DAC}, since the front-end achieves $8.3\,\mathrm{fC}$, as later demonstrated, using $Q = C \times V$ the capacitance is expected to be approximately $6.9\,\mathrm{fF}$. After optimization, the final dimensions are set to a W of $150\,\mathrm{nm}$ and L of $2.3\,\mu\mathrm{m}$, yielding $5\,\mathrm{fF}$. Finally, C_i is set with a W of $13\,\mu\mathrm{m}$ and L of $16\,\mu\mathrm{m}$, resulting in a total capacitance of $2.65\,\mathrm{pF}$.

7.2 Clock Generation

Clock generation is essential for synchronizing the various $\Sigma\Delta$M components. In the reference circuit, clock generation is provided externally, complicating testing the system, as seen in Chapter 5. A robust clock generation circuit is designed to meet strict requirements for low power consumption, area, and resilience to clock jitter and skew. The implementation utilizes a combination of logic gates from the TSMC $\mathrm{tcbn65gplus}$ standard cell library, which includes logic gates optimized with a small cell area [9].

The design draws inspiration from traditional dual-modulus three-times dividers to generate three non-overlapping clocks [64, 65]. Fig. 7.4 presents the topology and gate-level circuit schematic of the developed prescaler, which consists of three stages of D-Flip-Flops (DFFs) and a NOR gate. The NOR gate introduces additional time delay, which limits the operating frequency of the prescaler. As a result of this topology, to produce an output clock frequency of $15\,\mathrm{MHz}$, an input clock frequency of $45\,\mathrm{MHz}$ is required. Due to its feedback implementation, this design is free from bootup issues and is guaranteed to operate as expected after 3 clock cycles once powered.

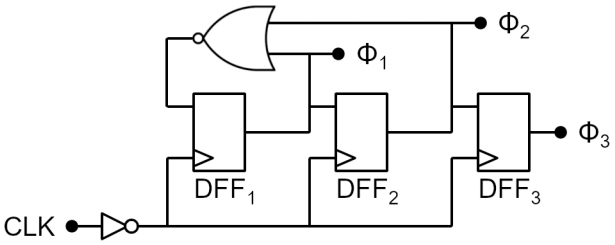


Figure 7.4: Clock Generator Base Circuit Schematic.

The complete design prioritizes basic cells such as NOTs, NORs, and NANDs to minimize transistor count and, thus, area utilization. The circuit includes a total of 3 DFFs, 3 NOTs, 2 NORs, 2 NANDs, and an AND gate. Each component has different versions based on its driving capability, and, for every case, the lowest possible setting is chosen to reduce both power consumption and area usage. This circuit generates the required three non-overlapping clocks, ϕ_1, ϕ_2, and ϕ_r, as well as the enable signal, which controls the g_m cell. Fig. 7.5 illustrates a time diagram representing the behavior of these waveforms.

In the $\Sigma\Delta$M, the signals ϕ_1 and ϕ_2 do not directly exist, but their negated forms are present as the boot-strapped switches operate using these inverted signals. With this consideration, the feedback control logic is adjusted to minimize both area and logic gate usage. From the expressions presented in Tab. 7.4, it is evident that $\bar{\phi}_{f1}$ is equivalent to ϕ_{f4}, and $\bar{\phi}_{f2}$ is equivalent to ϕ_{f3}. Since y and $\bar{y}$ are available from the differential

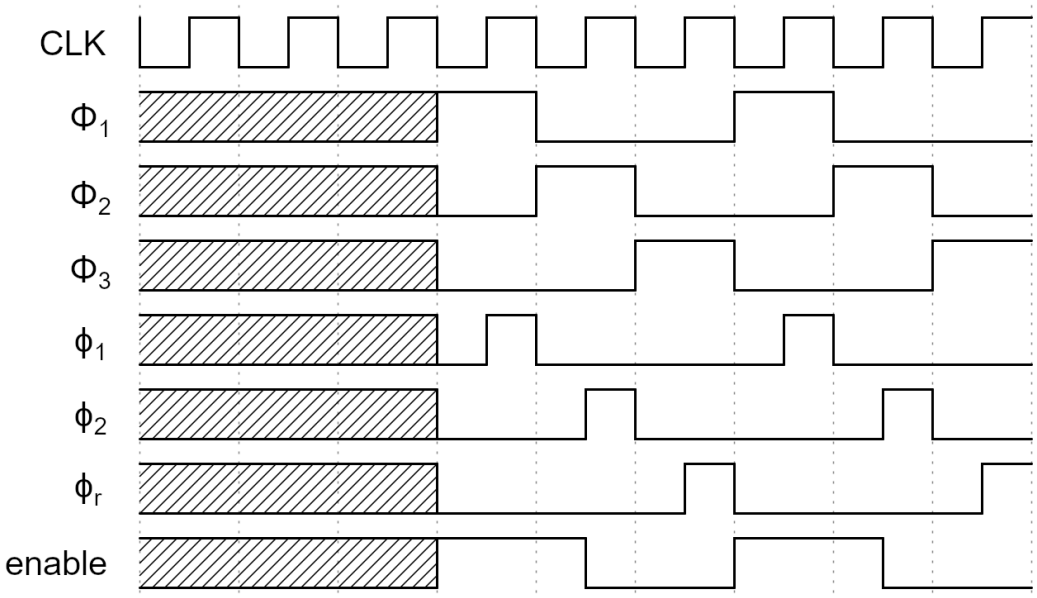


Figure 7.5: ΣΔM Control Clocks Representation.

implementation of the comparator, the feedback control clocks can be expressed in terms of y, $\bar{y}$, and $\bar{\phi}_1$, using NANDs or NORs, to optimize area and logic gate usage. This transformation, simplified using De Morgan's laws, requires only two NORs gates and two NOT gates.

Table 7.4: Functions for the Feedback Control Clocks.

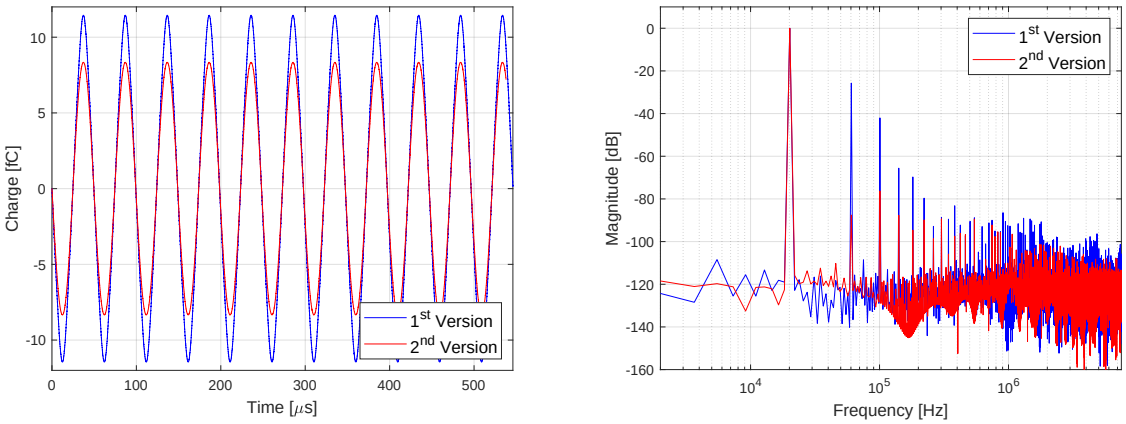
ϕ_{f1}	ϕ_{f2}	ϕ_{f3}	ϕ_{f4}
$y \wedge \phi_1$	$y \vee \bar{\phi}_1$	$\bar{y} \wedge \phi_1$	$\bar{y} \vee \bar{\phi}_1$
$\overline{\bar{y} \vee \bar{\phi}_1}$	$\bar{\phi}_{f3}$	$\overline{y \vee \bar{\phi}_1}$	$\bar{\phi}_{f1}$

7.3 Pre-Layout Simulations

The pre-layout simulations are essential for validating design choices and ensuring the circuit meets the specified operational parameters. This section details various simulations, including typical conditions testing, corner simulations, and MC simulations, for both the front-end and the complete and final version ΣΔM. In the conducted corner simulations, all combinations of process conditions and temperatures are tested. Furthermore, MC simulations, which assign individual values to each device, allow for a comprehensive inspection of how mismatch and process variations can impact performance. Together, these methodologies assist in identifying potential weaknesses in the design. The circuit test bench remains the same as described in Section 4.2, operating a transient simulation with a differential input signal of $200\,\mathrm{mV}$ amplitude at a frequency of $20141.6\,\mathrm{Hz}$ and a sampling frequency of $15\,\mathrm{MHz}$ under typical conditions. This sinusoidal signal is combined with a DC voltage set to half of the supply voltage, $600\,\mathrm{mV}$, to bias the g_m cell appropriately.

7.3.1 $\Sigma\Delta$M Front-End

The front-end output charge, presented in Fig. 7.6, is sampled at 8192 points to ensure coherent sampling and to prevent spectral leakage. This optimized version of the $\Sigma\Delta$M front-end achieves a differential charge per iteration with an amplitude of $8.34\,\mathrm{fC}$, resulting in a $17\,\%$ reduction compared to the previous $\Sigma\Delta$M version. This charge amplitude is used to appropriately size the feedback capacitor, as outlined in Sections 4.1.3 and 7.1.3. The front-end exhibits an ENOB of $12.05\,\mathrm{bit}$, which is three times higher than the first version due to the reduction of distortion introduced by odd harmonics, as confirmed by the DFT in Fig. 7.6(b), and is aligned with the reference $\Sigma\Delta$M result of $12.03\,\mathrm{bit}$ [28]. The improvement results from the enhanced linear gain region in the g_m cell and adapted MOSCAP sizes.



(a) Differential Charge Sine Signals

(b) Respective DFTs

Figure 7.6: Front-End Transient Simulation Comparison.

With these enhancements in the front-end design, it is essential to investigate how variations in process conditions influence performance. In this context, corner simulations are conducted, which account for different operating conditions categorized into typical, slow, and fast variations. The slow and fast variants are available in four combinations, as shown in Tab. 7.5. These combinations result in variations in μ and V_{th}. Additionally, the temperature is varied across three values: $-40\,^{\circ}\mathrm{C}$, $27\,^{\circ}\mathrm{C}$, and $125\,^{\circ}\mathrm{C}$.

Table 7.5: Variations in μ and V_{th} for Different Corner Cases.

Model	NMOS	PMOS
fast-fast	$\mu_n \nearrow \lvert V_{th}\rvert \searrow$	$\mu_p \nearrow \lvert V_{th}\rvert \searrow$
fast-slow	$\mu_n \nearrow \lvert V_{th}\rvert \searrow$	$\mu_p \searrow \lvert V_{th}\rvert \nearrow$
slow-fast	$\mu_n \searrow \lvert V_{th}\rvert \nearrow$	$\mu_p \nearrow \lvert V_{th}\rvert \searrow$
slow-slow	$\mu_n \searrow \lvert V_{th}\rvert \nearrow$	$\mu_p \searrow \lvert V_{th}\rvert \nearrow$

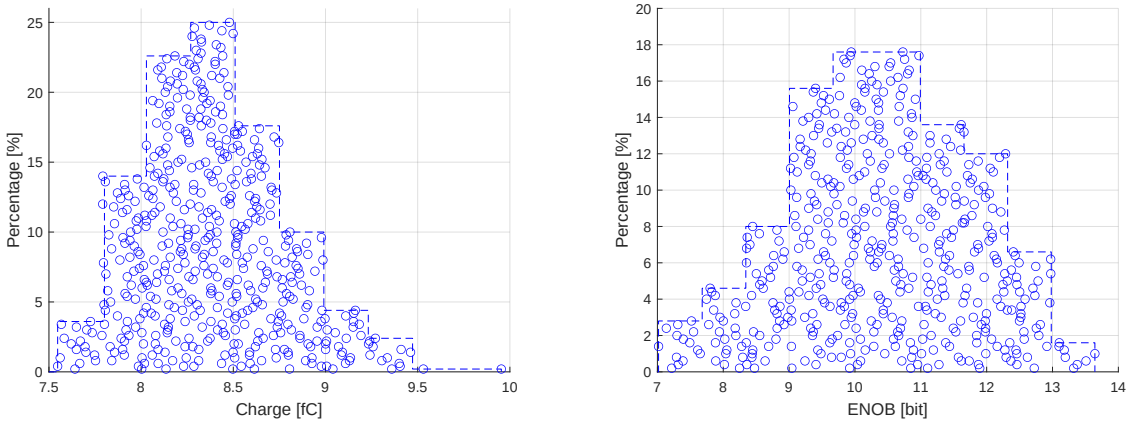
As stated in Section 3.2.1, the bias current of the g_m cell is significantly influenced by PVT variations. Changes in V_{th} result in corresponding variations in the drain currents, substantially affecting the g_m cell behavior. As a result, these variations are expected to impact the frond-end resolution considerably.

Tab. 7.6 presents all results for the aforementioned variations. The mean value for all tested cases for ENOB is $8.4\,\mathrm{bit}$, indicating a difference of almost $4\,\mathrm{bit}$ from the typical result. Several conclusions can be drawn. First, the fast-slow case exhibits the poorest performance among the combinations. Second, the variations in NMOS do not demonstrate significant differences in circuit performance compared to PMOS, with PMOS showing a more pronounced impact on performance. Finally, the slow-fast combination yields the best overall performance, as the values exhibit the least variation.

Table 7.6: Results for ENOB Across Different Corner Cases.

Model	**Temperature** [°C]	**ENOB** [bit]
fast-fast	-40	10.4
	27	10.7
	125	6.5
fast-slow	-40	6.5
	27	8.7
	125	6.8
slow-fast	-40	9.9
	27	9.2
	125	8.4
slow-slow	-40	6.3
	27	7.0
	125	10.4

To conclude the analysis of the $\Sigma\Delta$M front-end, MC simulations are conducted using 500 points, accounting for variations in mismatch, process, and both factors simultaneously. This number is chosen as a standard for such simulations, as it accounts for $99.7\,\%$ of the potential outcomes [66]. The statistical distributions for the maximum charge and the ENOB obtained from the simultaneous mismatch and process simulations are shown in Fig. 7.7.



(a) Maximum Differential Charge Distribution

(b) ENOB Distribution

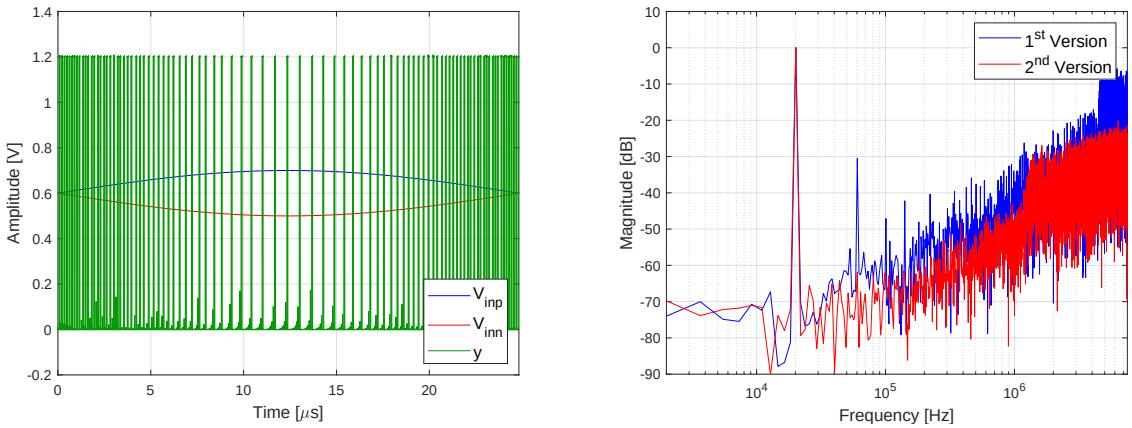
Figure 7.7: Statistical Distributions from the MC Simulations with both Mismatch and Process Variations.

The distribution shown in Fig. 7.7(a) is characterized by a mean of $8.39\,\mathrm{fC}$ and a standard deviation of $0.383\,\mathrm{fC}$. The charge value is intended to be static, and the low standard deviation is a favorable outcome. Furthermore, these values are consistent with typical results, supporting the use of the selected value for the dimensioning of C_{DAC}. Regarding the ENOB, depicted in Fig. 7.7(b), the mean is $10.35\,\mathrm{bit}$ with a standard deviation of $1.37\,\mathrm{bit}$. These results are within acceptable limits, as they exceed the theoretical ENOB of the $\Sigma\Delta$M, set at $9.64\,\mathrm{bit}$ [11, 17], leaving noise budget for the remaining blocks of the $\Sigma\Delta$M. The MC simulations for mismatch only and process only yield similar results. For instance, the process MC simulations result in a maximum charge mean value of $8.389\,\mathrm{fC}$ with a standard deviation of $0.529\,\mathrm{fC}$, and an ENOB mean value of $10.35\,\mathrm{bit}$ with a standard deviation of $1.36\,\mathrm{bit}$. Consequently, these results do not allow for a conclusion regarding whether mismatch or process variations have a more significant effect on performance.

7.3.2 Complete $\Sigma\Delta$M

The complete $\Sigma\Delta$M test bench remains unchanged from the version presented in Section 4.2, featuring an ideal output capacitor of $100\,\mathrm{fF}$. The output voltage node y of the $\Sigma\Delta$M is used to evaluate resolution by computing the DFT of the waveform, using 8192 points to ensure coherent sampling. Fig. 7.8 illustrates half a period of the input voltages to demonstrate the modulation effect and the resulting output DFT. The output y, shown in Fig. 7.8(a), is modulated by the input differential voltage, showing higher dependence on the input than the version in Section 4.2.

In this $\Sigma\Delta$M implementation, distortion from odd harmonics is minimal. The ENOB obtained from the spectrum, assuming an OSR of 128, is $9.01\,\mathrm{bit}$, representing an improvement of nearly $1\,\mathrm{bit}$ over the original result of $8.23\,\mathrm{bit}$ [28]. Additionally, the ENOB for this version is compared to the theoretical maximum ENOB for three different OSR values [17]. These results are summarized in Tab. 7.7, further confirming the effectiveness of this implementation in reducing harmonic distortion, as the results show minimal deviation.



(a) Input vs. Output Signals

(b) Output Signals DFT

Figure 7.8: Complete $\Sigma\Delta$M Differential Transient Simulation.

Table 7.7: ENOB Comparison for Different OSR Values.

OSR	128	64	32
Theoretical ENOB [bit]	9.64	8.14	6.64
Achieved ENOB [bit]	9.01	7.56	6.55

In terms of energy, the total power consumption of the complete $\Sigma\Delta$M measures $7.92\,\mu\mathrm{W}$. This result indicates a reduction in power consumption by a factor of 10 compared to the values presented by the reference $\Sigma\Delta$M, and a $32\,\%$ reduction from the initial implementation while generating the necessary control clocks and having higher complexity. Tab. 7.8 provides the power consumption for each building block, demonstrating that the g_m cell accounts for the largest portion at $35.7\,\%$ of the total power. This result reflects a reduction by a factor of 2.5 compared to the first implementation, with the results detailed in Section 4.2. Furthermore, this $\Sigma\Delta$M implementation exhibits a more balanced power distribution across the building blocks, with the three most demanding blocks having nearly identical power consumption.

Table 7.8: Power Distribution for the Final Version $\Sigma\Delta$M.

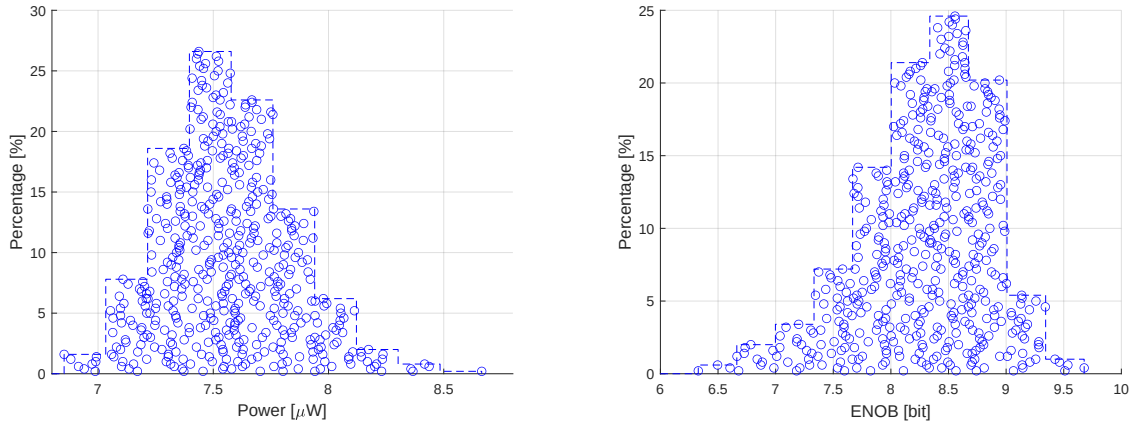
Building Block	**Power Consumption** [μW]	**Power Percentage** [%]
g_m Cell	2.83	35.7
Bootstrapped Switches	0.17	2.2
StrongARM Comparator	2.45	30.9
Clock Generation and Logic	2.47	31.2

Tab. 7.9 presents the results of the complete $\Sigma\Delta$M for the corner simulations. The mean value of ENOB across all cases is $8.19\,\mathrm{bit}$, representing a deviation of around $1\,\mathrm{bit}$ from the typical result. The fast-slow case shows the lowest resolution among the tested combinations, consistent with the front-end results. In contrast, the fast-fast combination achieves the highest resolution for the complete $\Sigma\Delta$M. Regarding power consumption, the fast-fast combination, also referred to as the worst-power corner, demonstrates the highest power consumption, while the slow-slow combination results in the lowest. As expected, power consumption increases with rising temperature.

Table 7.9: Results for Performance Across Different Corner Cases.

Model	**Temperature** [°C]	**ENOB** [bit]	**Power Consumption** [μW]
fast-fast	−40	9.3	8.6
	27	8.6	8.9
	125	8.1	11.4
fast-slow	−40	8.6	7.3
	27	8.4	7.5
	125	7.1	8.4
slow-fast	−40	7.4	7.5
	27	9.4	7.8
	125	8.4	8.5
slow-slow	−40	8.0	6.6
	27	8.2	6.8
	125	8.1	7.1

MC simulations are once again performed using 500 points, including variations in mismatch, process, and both factors simultaneously. The statistical distributions for power consumption and ENOB derived from the process-only simulations are presented in Fig. 7.9. The distribution in Fig. 7.9(a) shows a mean of $7.56\,\mu\mathrm{W}$ with a standard deviation of $0.27\,\mu\mathrm{W}$, which aligns with the typical results. For the ENOB, illustrated in Fig. 7.9(b), the mean is $8.29\,\mathrm{bit}$ with a standard deviation of $0.56\,\mathrm{bit}$, reflecting a reduction of $0.7\,\mathrm{bit}$ from the typical value. The MC simulations for both mismatch only and simultaneous mismatch and process variations produce comparable results, again providing no clear indication of whether mismatch or process variations have a more significant impact on performance.

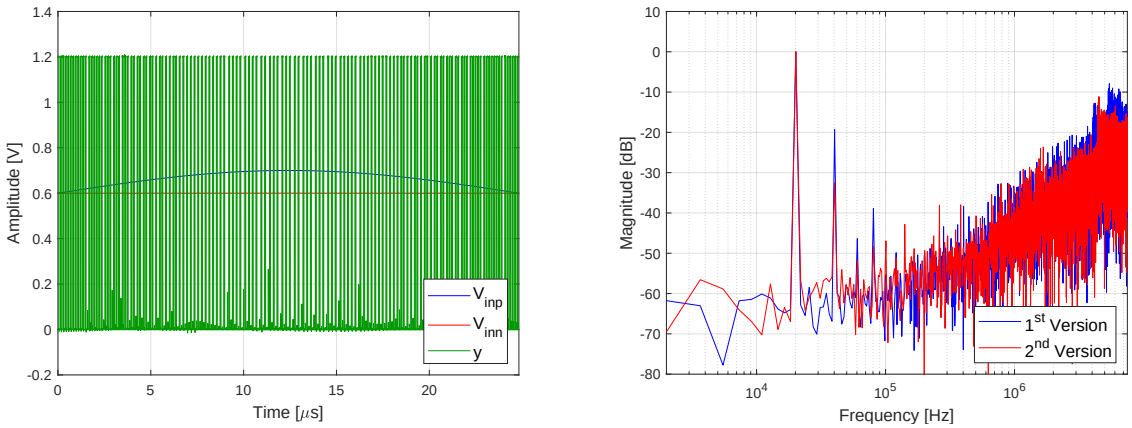


(a) Power Consumption Distribution

(b) ENOB Distribution

Figure 7.9: Statistical Distributions from the MC Simulations with only Process Variations.

A test is conducted using only one input, configuring the $\Sigma\Delta$M as a single-input system rather than a differential one, as done in Section 4.2. The results of this test are illustrated in Fig. 7.10.



(a) Input vs. Output Signals

(b) Output Signals DFT

Figure 7.10: Complete $\Sigma\Delta$M Single-Input Transient Simulation.

The output bit stream maintains a modulated appearance, but similar to the results in Section 4.2, the DFT shows second and third-order harmonics. This distortion results in an ENOB of $5.01\,\mathrm{bit}$ for an OSR of 128, representing a $79\,\%$ improvement over the initial implementation. Theoretically, for single-input operation, a SNDR reduction of $3\,\mathrm{dB}$ would be expected, leading to a corresponding ENOB reduction of $0.21\,\mathrm{bit}$ from the differential configuration. However, the observed reduction is larger in this case, indicating room for further improvement in the single-input mode.

7.4 Layout Optimizations

After optimization at the functional and logic levels, the focus shifts to physical design. The objective at this stage is to optimize the circuit layout for a minimal area while avoiding performance bottlenecks and ensuring compliance with the foundry's design rules, as discussed in Section 4.3. A significant challenge during this step is the management of the well proximity effect (WPE), a phenomenon derived from nonuniform well doping across the manufactured wafer, which results in higher V_{th} values for device wells located near the edge [67,68]. As noted in Sections 3.2.1 and 7.3.1, the g_m cell performance is susceptible to changes in this parameter. The WPE is modeled in simulations using the parameters SCA, SCB, and SCC, which depend on the layout geometries of the transistor and the proximity of well edges [68]. While detailed analysis of these parameters is beyond the scope of this work, evaluating their effects is critical, and efforts are made to minimize them in the g_m cell. Chapter B presents the various implementations explored throughout the design process, along with the corresponding SCA, SCB, and SCC parameters obtained from the PEX process. The design modifications discussed in Section 7.1 and subsequent layout iterations result in the layout depicted in Fig. 7.11, where the various components are labeled. The layout dimensions are $29.9\,\mu\mathrm{m}$ by $35.6\,\mu\mathrm{m}$, resulting in a total active area of $1068\,\mu\mathrm{m}^2$.

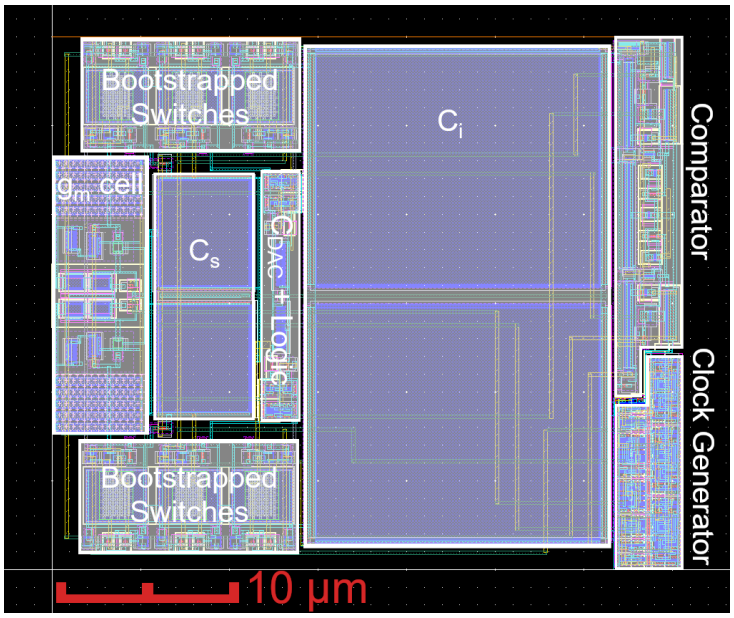


Figure 7.11: Final ΣΔM Version Layout Implementation.

In this version, the pads are all positioned on the same side, with an additional $10\,\mu m$ of distance between each, as shown in Fig. 7.12. The $\Sigma\Delta$M is highlighted by a white frame. This configuration has a notable advantage over the first version presented in Section 4.3, as it contains three fewer pads, significantly simplifying the layout. The circuit measures $177\,\mu m$ by $736\,\mu m$, resulting in a total area of $0.130\,mm^2$.

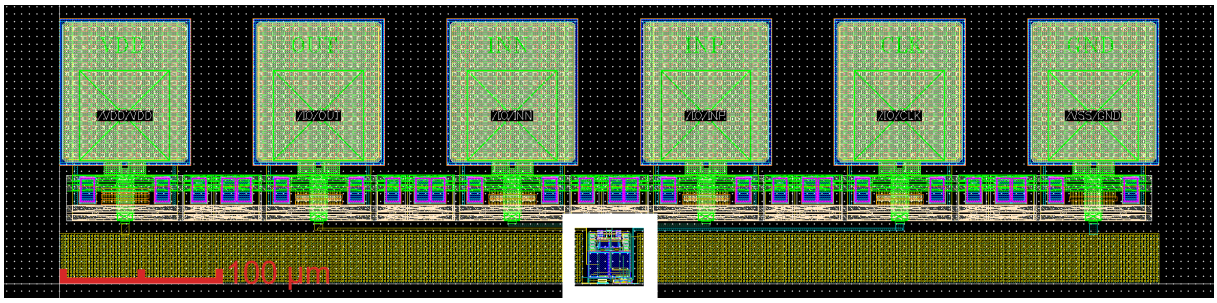


Figure 7.12: Final $\Sigma\Delta$M Version Layout Implementation with Pads.

The achieved areas are compared to those detailed in Section 4.3. Similar to the previous area analysis, a comparison is made of the percentage of area occupied by each building block. Tab. 7.10 summarizes this data, using the same symbology as presented in Section 4.3.

Table 7.10: Area Comparison and Distribution of the Final $\Sigma\Delta$M Version.

Building Block	**Original Area** [μm^2]	**1st Version Area** [μm^2]	**2nd Version Area** [μm^2]	**Area Percentage** [%]
g_m Cell	40	169.2	82.6 (2×↘)	7.7
MOSCAPs	1440	884.2	580.0 (1.5×↘)	54.3
Bootstrapped Switches	-	354.3	158.6 (2.2×↘)	14.9
StrongARM Comparator	400	84.5	72.1 (1.2×↘)	6.8
Control Logic	400	67.3	16.3 (4.1×↘)	1.5
Clock Generation	-	-	42.7	4.0
Complete $\Sigma\Delta$M	2400	1735	1068 (1.6×↘)	100

Some conclusions can be drawn at this stage. The final version exhibits increased complexity and improved resolution under typical conditions, along with a reduction of 2.3 times in terms of area. As expected, the MOSCAPs continue to be the largest contributors to the total chip area, accounting for $54.3\,\%$. Finally, as indicated in Tab. 7.10, approximately $12\,\%$ of the area remains unoccupied or is used for interconnect purposes. This result represents a 2 times reduction in the actual unoccupied area compared to the previous version, indicating high compactness for the final design.

7.5 Post-Layout Results

Post-layout simulations are conducted to confirm that the parasitics introduced do not significantly impact performance. The PEX simulations verify that the design is prepared for tape-out, as similarly addressed in Section 4.4. The layout in Fig. 7.11, without pads, achieves an ENOB of $8.2\,bit$, reflecting a reduction of $0.8\,bit$. Power consumption increases by $1.5\,\mu W$, resulting in a total of $9.42\,\mu W$ under typical conditions. The addition of circuit pads does not substantially affect the resolution of the $\Sigma\Delta$M, reducing the ENOB to $7.9\,bit$, while

power consumption reaches $10.2\,\mu\mathrm{W}$. The limited impact of layout parasitics on performance is attributed to careful layout optimization, incorporating the insights gained throughout the different design processes.

A standard analysis is presented in Fig. 7.13, illustrating the relationship between SNDR and input amplitude. The peak SNDR values recorded are $67\,\mathrm{dB}$ and $64\,\mathrm{dB}$ for the $\Sigma\Delta$M under typical conditions pre- and post-layout simulations, respectively. These values are obtained for an input differential amplitude of $-2.5\,\mathrm{dBFS}$ or $225\,\mathrm{mV}$.

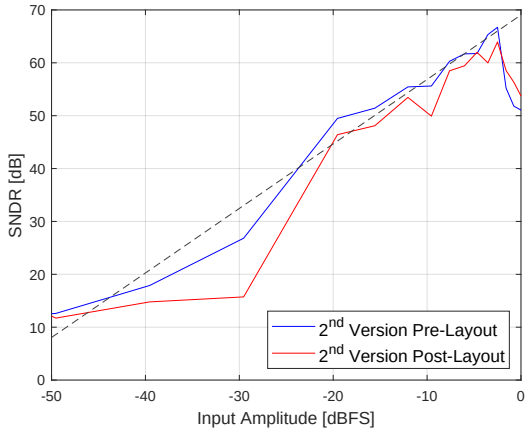


Figure 7.13: Measured SNDR vs. Input Amplitude Analysis of the Final $\Sigma\Delta$M Version.

The performance of the designed circuit is compared with those presented in Section 2.5, as well as all modulator versions discussed in this document. The shown results correspond to the pad-less post-layout final $\Sigma\Delta$M version. The relationship between area and power, illustrated in Fig. 7.14, demonstrates that the developed $\Sigma\Delta$M is the smallest $\Sigma\Delta$ converter among the surveyed circuits [14].

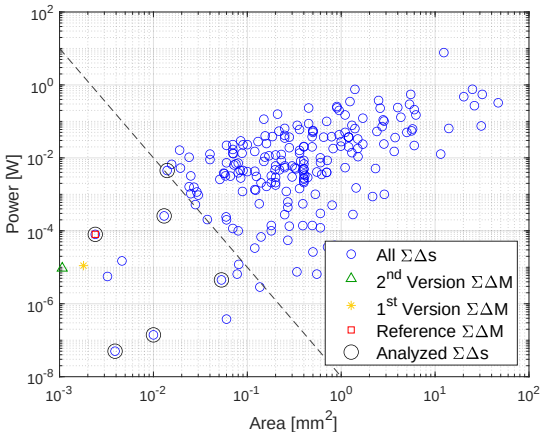
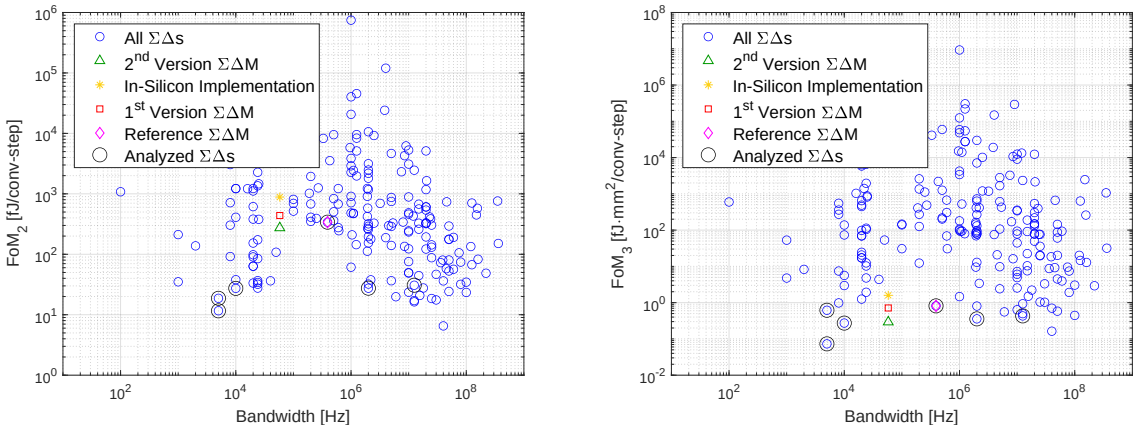


Figure 7.14: Area vs. Power Consumption Analysis considering $\Sigma\Delta$ Converters.

Next, the FoM$_2$ and FoM$_3$ values are calculated, yielding $273.4\,\mathrm{fJ/conv-step}$ and $0.292\,\mathrm{fJ\cdot mm^2/conv-step}$, respectively. These results, depicted in Fig. 7.15, indicate an improvement of $20\,\%$ in FoM$_2$, while FoM$_3$ shows a reduction by a factor of 2.8. Although FoM$_2$ is reduced compared to the reference $\Sigma\Delta$M, it remains above the acceptable value of $20\,\mathrm{fJ/conv-step}$ defined in Section 2.5.4. For the FoM$_2$ to fall within an acceptable range,

it must be further reduced by a factor of 14. This reduction can be accomplished through a combination of enhancements in resolution, power consumption, and adjustments to sampling frequency. Attaining a satisfactory FoM_2 appears feasible with the proposed design, although it requires significant time investment. Nevertheless, the work presented in this thesis emphasizes minimizing area, which is successfully accomplished, thereby addressing the gap in $\Sigma\Delta$ converters for the bandwidth range of $25\,\text{kHz}$ to $350\,\text{kHz}$, ensuring a competitive FoM_3 within this range.



(a) FoM_2 **(b)** FoM_3

Figure 7.15: FoMs vs. Bandwidth Analysis considering $\Sigma\Delta$ Converters.

At last, the performance metrics are summarized in Tab. 7.11. This section concludes the thesis work, with the contributions and potential future research directions outlined in the following chapter.

Table 7.11: Final $\Sigma\Delta$M Performance Metrics.

Technology [nm]	65
Area [μm^2]	1068
Supply Voltage [V]	1.2
Samp. Frequency [MHz]	15
Bandwidth [kHz]	58.59
ENOB [bit]	8.2
Power Consumption [μW]	9.42
FoM_2 [fJ/conv-step]	273.35
FoM_3 [$\text{fJ}\cdot\text{mm}^2/\text{conv-step}$]	0.29

Chapter 8

Conclusion

In this thesis, a low-area, low-power $\Sigma\Delta$M, designed for integration into OoC systems with a specific focus on UC3 of the UNLOOC project, is successfully developed, taped-out, tested, and optimized using the $65\,\mathrm{nm}$ TSMC technology. The resulting circuit enhances the FoMs of the reference design while addressing the gap in efficient small $\Sigma\Delta$ converters for the needed bandwidth.

This final chapter shows the general conclusions of the work, along with the main challenges and directions for future research.

8.1 Achievements

The work presented accomplishes several objectives. The following points summarize the most significant achievements throughout the project:

- Chip Manufacturing: Familiarity with the tape-out procedure is developed, encompassing the preparation and submission process required to manufacture the IC. This development facilitates a smoother transition from design to silicon implementation in the final $\Sigma\Delta$M design;
- Design Validation: The original modulator topology undergoes validation by testing the manufactured circuit. This validation confirms that the design meets the expected resolution and power consumption;
- Workflow Improvement: Significant simulation workflow improvements occur. By optimizing this process, it becomes possible to conduct MC simulations with the required number of points and to include parasitic simulations that would otherwise take months to perform;
- Compact Area: The final design achieves a notable reduction in area, measuring $1068\,\mu\mathrm{m}^2$, which is 2.3 times smaller than the original version [28]. The developed $\Sigma\Delta$M is the smallest $\Sigma\Delta$ converter among the surveyed circuits [14], reinforcing its suitability for miniaturized applications. The square geometry also provides advantages as it is compatible with large sensor matrices;

- Adequate Resolution: The final version of the modulator achieved an ENOB of $8.2\,\mathrm{bit}$, with minimal resolution degradation attributed to parasitic effects from the layout process;
- Power Efficiency: The modulator demonstrates a low power consumption of $9.42\,\mu\mathrm{W}$, which is suitable for the power-constrained environment of OoC applications. This represents an improvement of 8.5 times compared to the reference $\Sigma\Delta$M [28], ensuring reliable operation without introducing thermal stress;

8.2 Key Challenges

The design of the $\Sigma\Delta$M presented some difficulties. The available documentation on the original $\Sigma\Delta$M primarily addressed system functionality, with a limited focus on performance metrics such as area and power consumption. This lack of information required additional contact with the $\Sigma\Delta$M authors and further research, which delayed the development of the improved version and left gaps in comparisons, as discussed in Chapter 3. The layout process for the ported version, outlined in Chapter 4, introduces additional challenges due to the integration of circuit pads, which has limited coverage in coursework and requires some design considerations. Wire bonding posed further trouble, especially in avoiding short circuits, as outlined in Chapter 5. Additionally, the original workflow could have been more optimally organized, prompting the need for a more efficient simulation process, as described in Chapter 6. Reducing parasitic effects in the final layout, mainly in Chapter 7, necessitated iterative refinement and optimization.

8.3 Future Work

The first item in the future work involves increasing the ENOB to exceed $10\,\mathrm{bit}$. Achieving this requires an OSR greater than 151 using the proposed architecture [17]. Further optimization can be accomplished by refining the circuit layout and addressing parasitic effects through techniques such as the use of dummy transistors [68, 69] or modifications to the front-end architecture, with particular emphasis on the g_m cell [34–37]. Moreover, enhancement of the FoM_2 is identified as another area of improvement.

The final $\Sigma\Delta$M design already occupies a significantly smaller area than other ADCs. One method to further reduce the area is to adopt more advanced CMOS processes with smaller transistor dimensions. Since the employed topology does not utilize amplifiers, the impact of short-channel effects is expected to be negligible.

The fabrication of the developed circuit is necessary to validate its performance and identify design issues related to temperature dissipation, which are critical to its intended application. Due to the time constraints of a master's thesis, fabricating and testing multiple circuits is not feasible, as this process typically takes several months. However, the final $\Sigma\Delta$M is prepared for fabrication, which is expected to occur during the tape-out run in December 2024. Additionally, incorporating testability features in the design would enable more efficient debugging and a better understanding of discrepancies between experimental and simulation results. A custom PCB must also be designed to effectively test such $\Sigma\Delta$Ms.

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Appendix A

SKILL Script

This appendix presents in Listing A.1 the script mentioned in Section 6.5, which can be utilized for any pair of cell and cell view within the same library. This script executes simulations sequentially, ensuring that only one core is utilized to minimize conflicts between users, enhance resource efficiency, and prevent crashes.

Listing A.1: script.il File.

```
simulations = list(
    ; Use ";" to comment the not needed simulations
    list("IH_tb" "adexl_corners"),
    list("IH_tb" "adexl_mmp"),
    list("IH_tb" "adexl_mm"),
    list("IH_tb" "adexl_p"),
    list("MODULATORNC_tb" "adexl_corners"),
    list("MODULATORNC_tb" "adexl_mmp"),
    list("MODULATORNC_tb" "adexl_mm"),
    list("MODULATORNC_tb" "adexl_p"),
    list("MODULATOR_tb" "adexl_base"),
    list("MODULATOR_tb" "adexl_corners"),
    list("MODULATOR_tb" "adexl_mmp"),
    list("MODULATOR_tb" "adexl_mm"),
    list("MODULATOR_tb" "adexl_p"),
    list("MODWPADS_tb" "adexl_base"),
    list("MODWPADS_tb" "adexl_corners")
    ; ...
)

; Variable Initialization
currentSimIndex = 0

```

```
; Main Routine
procedure(runNextSimulation()
    if(currentSimIndex < length(simulations) then
        ; Name Parsing
        sim = nth(currentSimIndex simulations)
        tbName = car(sim)
        setupName = cadr(sim)

        ; Simulation Setup and Running
        axlSess = axlCreateSession(getCurrentTime())
        axlSetMainSetupDBLCV(axlSess "MODULATOR" tbName setupName)
        axlRunSimulation(?session axlSess ?callback "runNextSimulation()")

        printf("Running simulation %d: %s %s\n" currentSimIndex tbName setupName)
        currentSimIndex = currentSimIndex + 1
    else
        printf("All simulations completed.\n")
        exit()
    )
)

runNextSimulation()
```

Appendix B

g_m Cell Layout Comparison

This appendix compares various g_m cell layouts, emphasizing differences in key parameters such as transconductance, bandwidth, and dynamic range. Each layout is evaluated to assess the impact of geometry on performance.

Fig. B.1 illustrates the structure of layout 1. As outlined in Section 7.1.1, the parameters SCA, SCB, and SCC represent non-idealities and are ideally equal to 0 [67, 68]. Tab. B.1 provides the circuit geometry parameters for layout 1, with transistors labeled according to the schematic in Fig. 7.1. Based on SCA, SCB, and SCC values, this implementation is expected to demonstrate poor performance.

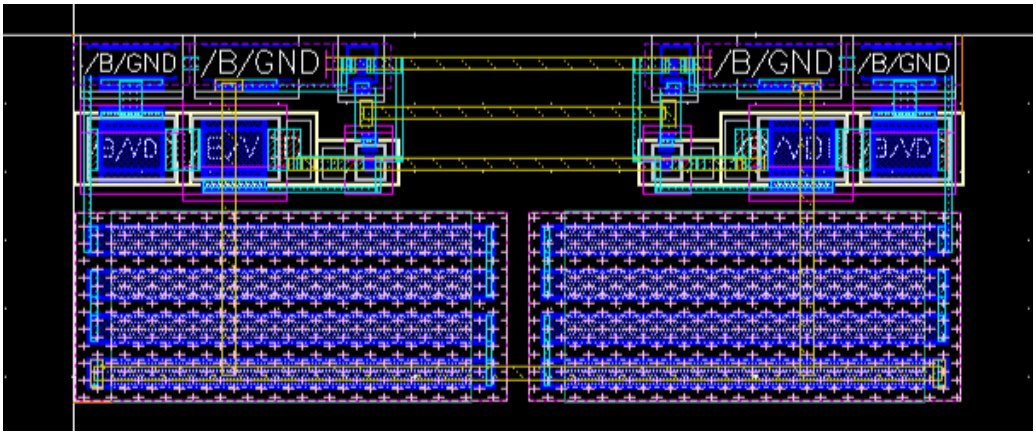


Figure B.1: 1st g_m Cell Layout Implementation.

Table B.1: 1st g_m Cell Layout Transistors Geometry Parameters.

Transistors	$P_{1,2}$	$P_{3,4}$	$N_{1,2}$	$N_{3,4}$
SCA	1.3×10^{1}	1.2×10^{1}	9.7	7.9
SCB	1.3×10^{-2}	1.2×10^{-2}	8.1×10^{-3}	7.1×10^{-3}
SCC	5.6×10^{-4}	5.5×10^{-4}	1.3×10^{-4}	1.2×10^{-4}

Tab. B.2 compares measured parameters such as DC gain, bandwidth, dynamic range, transconductance, and voltage noise for layout 1. The results show significant differences from the performance metrics in Tab. 7.3 in Section 7.1.1.

Table B.2: 1st g_m Cell Layout Performance Metrics.

A_0 [dB]	**Bandwidth** [MHz]	**Dynamic Range** [mV]	G_m [µS]	V_n [nV]
0.2	8.0	494.6	25.8	81.92

Fig. B.2 displays the layout 2, while Tab. B.3 details the circuit element geometry parameters for this layout. Notable reductions in the NMOS transistor spatial factors are observed, contributing to improved overall performance compared to layout 1, as shown in Tab. B.4.

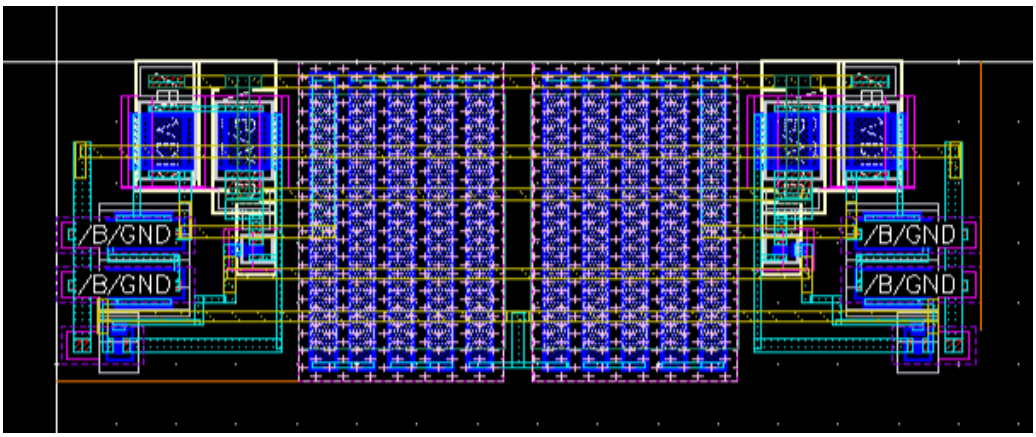


Figure B.2: 2nd g_m Cell Layout Implementation.

Table B.3: 2nd g_m Cell Layout Transistors Geometry Parameters.

Transistors	$P_{1,2}$	$P_{3,4}$	$N_{1,2}$	$N_{3,4}$
SCA	8.5	6.9	2.6	1.3
SCB	6.9×10^{-3}	5.9×10^{-3}	4.2×10^{-4}	1.1×10^{-6}
SCC	2.9×10^{-4}	2.8×10^{-4}	4.3×10^{-9}	4.6×10^{-10}

Table B.4: 2nd g_m Cell Layout Performance Metrics.

A_0 [dB]	**Bandwidth** [MHz]	**Dynamic Range** [mV]	G_m [µS]	V_n [nV]
0.8	7.9	544.2	27.6	81.93

Fig. B.3 illustrates the layout 3, while Tab. B.5 summarizes the corresponding transistors geometry parameters. This layout is optimized for higher performance, with smaller spatial factors minimizing layout-related WPE. This improvement is reflected in the enhanced performance metrics shown in Tab. B.6, where layout 3 achieves the highest G_m value, dynamic range, and gain, with differences of less than $5\,\%$ compared to the results in Tab. 7.3.

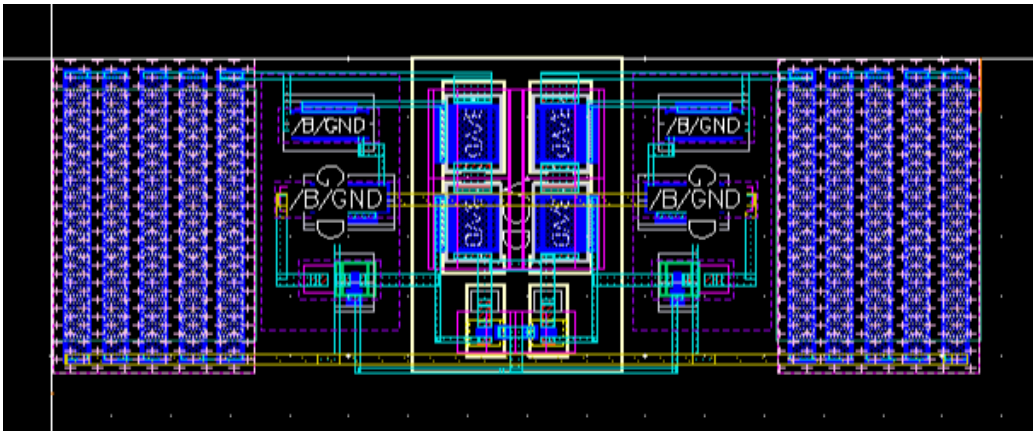


Figure B.3: 3rd g_m Cell Layout Implementation.

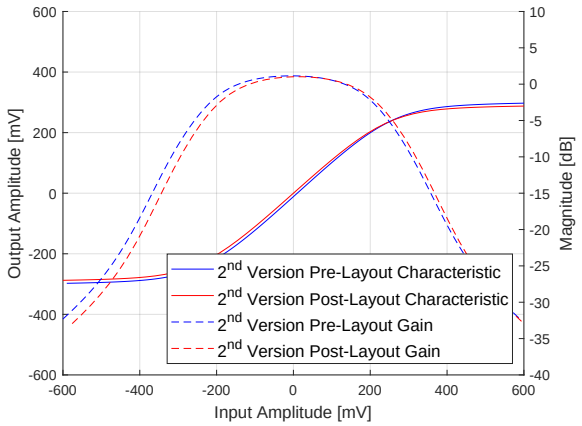
Table B.5: 3rd g_m Cell Layout Transistors Geometry Parameters.

Transistors	$P_{1,2}$	$P_{3,4}$	$N_{1,2}$	$N_{3,4}$
SCA	2.0	1.5	1.5	1.5
SCB	1.2×10^{-4}	9.3×10^{-5}	2.4×10^{-5}	2.0×10^{-4}
SCC	3.3×10^{-8}	3.0×10^{-8}	6.1×10^{-10}	2.4×10^{-7}

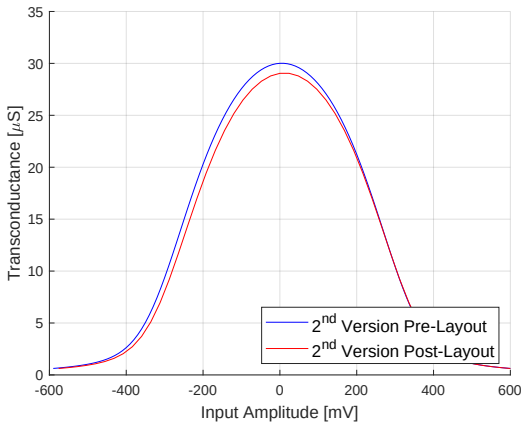
Table B.6: 3rd g_m Cell Layout Performance Metrics.

$\boldsymbol{A_0}$ [dB]	**Bandwidth** [MHz]	**Dynamic Range** [mV]	$\boldsymbol{G_m}$ [µS]	$\boldsymbol{V_n}$ [nV]
1.02	8.0	575	29.1	86.9

Fig. B.4 provides a visual comparison of the DC characteristics for layout 3 before and after layout simulation. The similarities between the pre- and post-layout results are consistent with the geometry and performance parameters.



(a) DC Transfer Function and Gain



(b) Transconductance vs. Input Voltage

Figure B.4: g_m Cell DC Characteristics Implementation Comparison.